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Small pitch 3D devices

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3D sensors are a promising option for the innermost pixel layers at the High Luminosity LHC. However, the required very high hit-rate capabilities, increased pixel granularity, extreme radiation hardness, and reduced material budget call for a device downscale as compared to existing 3D sensors, involving smaller pitch (e.g., 50×50 or 25×100 μm^2), shorter inter-electrode spacing (~30 μm), narrower electrodes (~5 μm), and reduced active thickness (~100 μm). The development of a new generation of 3D pixel sensors with these challenging features is under way by many research groups, in collaboration with processing facilities like FBK, CNM, and SINTEF. This paper talk will review the lessons learned from existing 3D detectors, and will address the main design and technological issues for small pitch 3D devices. Preliminary results from the electrical and functional characterization of the first prototypes will be reported and compared to TCAD simulations.

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1. Introduction

The ATLAS Insertable B-Layer (IBL) project led to an impressive progress in 3D radiation sensors, with experimental confirmation of their remarkable radiation tolerance with relatively low power dissipation, and the demonstration of medium volume productions with an acceptable yield [1, 2]. These accomplishments paved the way for using 3D sensors in other pixel detector systems in Phase 1 upgrades at the LHC (e.g., AFP [3] and CT-PPS [4]), and made them an appealing option also for the innermost tracking layers at the High Luminosity LHC (HL-LHC). The latter application will require very high hit-rate capabilities, increased pixel granularity, extreme radiation hardness (up to a fluence of 2×10^{16} n_{eq}/cm^2), and reduced material budget. Compared to existing 3D sensors, the future ones will have to be geometrically downscaled by about a factor of two, involving smaller pitch (e.g., 50×50 or 25×100 μm^2), shorter inter-electrode spacing (~30 μm), narrower electrodes (~5 μm), and reduced active thickness (~100 μm). The development of a new generation of 3D pixel sensors with these challenging features is under way by many research groups, in collaboration with processing facilities like FBK (Trento, Italy), CNM (Barcelona, Spain), and SINTEF (Oslo, Norway), and in parallel with a major effort from the CERN RD53 Collaboration aimed at a new pixel read-out chip (ROC) [5].

In this paper, lessons learned from existing 3D detectors are first briefly discussed, and the main design and technological issues relevant to small pitch 3D devices are analysed. Preliminary results from present R&D activities are summarized, with emphasis on the most recent developments within the INFN-FBK "Phase 2" Project.

2. Lessons learned from existing 3D detectors

The most significant experience with 3D detectors used so far in High Energy Physics experiments came with the ATLAS IBL project, for which a sensor production was carried out for the first time at FBK and CNM [2]. The tight IBL time schedule made evident that the double-sided 3D sensor technologies of FBK [6] and CNM [7] offered a number of advantages, among them reduced process complexity and faster production times compared to the single-sided 3D sensor technology with support wafer originally proposed at SNF (Stanford, USA) [8] and later transferred to SINTEF [9]. Furthermore, with double-sided 3D's the bias can be applied from the sensor back-side, making the front-side layout less demanding and significantly simplifying the sensor assembly within a pixel detector system. Although active edges are not feasible with double-sided 3D's, due to the lack of a support wafer, very compact slim edges (~100 μm or lower) can be implemented, that are good enough for most applications [10]. Nevertheless, without a support, wafers are more fragile, and mechanical yield is an issue: great care must be taken, especially in wafer edge protection. Moreover, wafer bowing can be pronounced: it can affect lithographical alignment quality and, if it exceeds 50 μm, it can compromise the feasibility of bump bonding. As a worst case, if coupled to high temperature process steps, it can also affect the electrical characteristics of the sensors and the fabrication

yield. In order to prevent this effect, the sensor front-side must be kept as "symmetric" as possible to the back-side through the entire process sequence.

Regardless of the specific approach and in spite of the significant advancement in the past few years, 3D sensor technology still remains quite complicated: critical process steps like Deep Reactive Ion Etching (DRIE) can induce major, irreversible damage, and the related defects are not easy to spot by standard techniques like optical inspection, since they can also be hidden deep in the bulk. Therefore, an accurate electrical characterization at wafer level is necessary to identify bad pixel sensors at an early stage, before bump bonding. To this purpose, the I-V measurement technique based on a temporary metal layer introduced at FBK for the IBL project proved to be effective and reliable [11].

3. Small pitch columnar devices

3.1 Viable technological approaches

An enhanced double-sided approach (Fig. 1a) has been developed by CNM for small pitch 3D sensors [12], but a minimum wafer thickness of ~200 μm is required due to mechanical fragility considerations. This is compatible with 4-inch diameter wafers, but it is too thin for 6-inch diameter ones. Since the electrodes are dead regions, in order for their volume to be minimized, a higher aspect ratio (depth/width) should be achieved for column etching: in ATLAS IBL sensors the aspect ratio was ~20:1, for small pitch sensors it should be increased to ~30:1. To this purpose, cryogenic DRIE techniques could be exploited [13].

As discussed in Section 2, a double-sided approach would offer several advantages: it is a more established process; the front side layout is less dense, a relevant feature for small pitch devices; the back-side sensor bias option comes for free; allowing the processing of ~200 μm active thickness, the signal charge for small tilted particles remains high. Among disadvantages are: the mechanical fragility (yield); the limited accuracy (a few μm) of the alignment between the front- and back-side of the wafers, that could be critical for small pitch sensors; the larger geometrical capacitance, and the larger pixel clusters for high tilt particles, due to the active thickness.

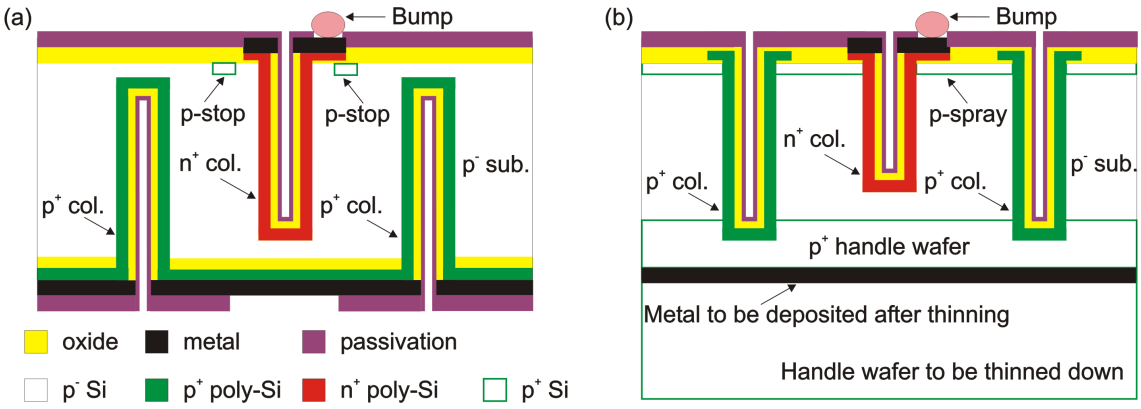

Figure 1 Schematic cross-sections of small pitch 3D sensors: (a) double-sided, and (b) single-sided.

As an alternative, a single-sided 3D technology with handle wafer has been proposed by FBK with modifications allowing for back-side sensor bias. As an example, Fig. 1b shows a device fabricated on Silicon Silicon Direct Wafer Bonded (Si-Si DWB) substrates from IceMOS Technology Ltd. (Belfast, North Ireland). These substrates consist of a Float Zone high-resistivity layer of the required thickness directly bonded (i.e., without an oxide layer in between) to a thick low-resistivity handle wafer. The p^+ (ohmic) columns are etched deep enough to reach the highly doped handle wafer, so that a good ohmic contact is achieved on the sensor back-side: the latter can eventually be partially thinned with a post processing and a metal layer can be deposited to ease the sensor bias. The high doping of the handle wafer also requires the etching of the n^+ (read-out) columns to be stopped a short distance (~20 μm) from it, in order to prevent from an early breakdown. Previous studies proved that such a structure with partially-through columns can yield relatively high breakdown voltage values, both before and after irradiation [14]. FBK also demonstrated the feasibility of this technology with Silicon on Insulator (SOI) wafers: to this purpose, it was proved that the p^+ columns can be etched by DRIE also through the bonding oxide, thus reaching the heavily doped handle wafer [15].

Among the advantages offered by the single-sided solutions are the mechanical robustness provided by the thick handle wafer, which is also compatible with active edges; moreover, the active layer thickness can be tailored to the desired value. With a thin active layer (~100 μm), narrow columns can be etched even though the aspect ratio is not improved, and all the device dimensions can be more easily downscaled. Among disadvantages is the extra effort and cost of post processing for handle wafer thinning and back-side metal deposition; moreover, the front side layout can become quite dense for small pitch sensor, as will be shown in the following.

An interesting modified single-sided technology for 3D thin sensors has been proposed by CNM. The process is very similar to the originally developed at SNF on SOI substrates, but it is completed by a local (i.e., patterned with a mask) wet etching of the handle wafer and a metal deposition in order to access the back-side of the active layer for sensor bias [16].

3.2 Pixel layouts: geometrical constraints

The layout of small pitch 3D sensor is straightforward, provided the device geometries are all downscaled. In this respect, the main problem for single-sided 3D pixels is due to the bump-bonding pad, whose size cannot be significantly reduced (see Fig. 2, referring to FBK technology with 5 μm column diameter and 20 μm bump pad diameter). In case of the 50×50 μm^2 pixel cell size (Fig. 2a) the bump pad can be safely placed far enough from the columns; this is also the case for the 25×100 μm^2 with one read-out electrode (1E, Fig. 2b). However, in the latter the inter-electrode spacing (L) is ~51.5 μm, that is not small enough for high radiation hardness. This can be improved with the design of two read-out electrodes (2E, Fig. 2c), yielding L~28 μm, however the layout becomes more critical because the bump pad is very close to both the read-out and the ohmic columns. As a result, this layout is sensitive to lithography misalignments of a few μm, that are typically achieved with mask aligners. The use of a better lithography system, e.g., a stepper with a submicron resolution, would of course

improve this aspect. Another solution being investigated is to place the bump pads directly on top of the columns, saving space all around [17].

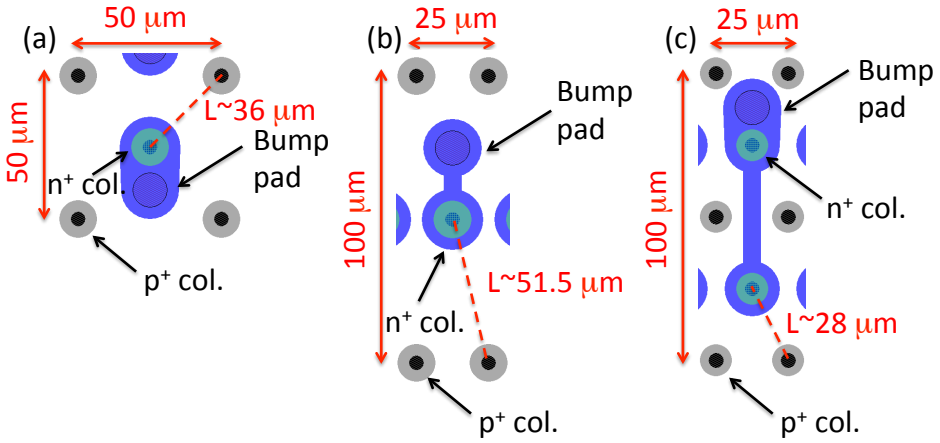

Figure 2 Layout of small pitch 3D pixels made with single-sided FBK technology: (a) 50×50 µm², (b) 25×100 µm² (1E), and (c) 25×100 µm² (2E).

Hosting the bump pad within a small pitch pixel is less critical in case of double-sided 3D processing technology, although the dead volume due to the columns is larger (e.g., in CNM technology the column diameter is 8 µm [12]) and the front-back alignment is worse. In fact, it should be noted that p^+ columns do not reach the front-side (see Fig. 1a), so that the bump pad can be placed very close or even overlap them without any risk of shorts or micro discharges.

4. Current R&D projects on 3D prototyping

4.1 The INFN-FBK "Phase 2" project

An ATLAS-CMS joint research activity in collaboration with FBK started in 2014, funded by INFN Scientific National Committee of particle physics (CSN1), and aimed at the development of new thin, small pitch pixel detectors for the HL LHC Phase-2 upgrades [15,18]. The program is concerned with both 3D and planar active-edge pixel sensors to be made on 6" p-type wafers. Here we only focus on 3D sensors. From the beginning, an extensive TCAD simulation activity has been carried out in order to optimize the device design. As a main outcome of this work, it was predicted that a capacitance of ~50 fF per read-out column and a breakdown voltage higher than 150 V can be achieved before irradiation, good enough for the planned application. As far as the signal efficiency after irradiation is concerned, by implementing into the simulation the new "Perugia" radiation damage model [19], both the 50×50 µm² and 25×100 µm² (2E) pixel layouts were found to yield very high average values, in the range from 60 to 70% after the largest possible irradiation fluence of 2×10^{16} n_{eq}/cm^2, thus anticipating the excellent radiation tolerance of such devices [17].

In parallel with the design/simulation activity, Si-Si DWB substrates of two different active thicknesses (100 and 130 µm) have been qualified by processing a batch of planar sensors [15,18]. A low leakage current was measured (~ a few nA/cm²), evidence of a good substrate

quality in terms of carrier generation lifetimes. Moreover, a significant diffusion (~10 μm deep) of Boron from the highly doped handle wafer into the active layer was also evaluated from C-V measurements, and confirmed by Secondary Ion Mass Spectroscopy (SIMS) measurements performed on a test wafer. As a result, the read-out column etching depth should be calibrated against the effective depth of the active layer in order to avoid an early breakdown.

The feasibility of the most critical process steps (e.g., the column etching by DRIE and their partial filling with poly-Si) was also proved at FBK [20]. In particular, column etching deeper than 150 μm was achieved, while maintaining a column diameter as narrow as 5 μm (aspect ratio > 30:1). Different etching recipes were developed for ohmic columns (optimized for larger depth) and read-out columns (optimized for better width uniformity).

The first batch of these new 3D sensors, consisting of 10 wafers, was processed at FBK with a wafer layout accommodating a large variety of sensors and test structures, as shown in Fig. 3a. Most of the wafer layout is dedicated to pixel sensors of both small pitch and standard pitch, compatible with existing ROCs like the ATLAS FE-I4 and the CMS PSI46dig. Some other smaller sensors are instead compatible with new small-pitch ROC prototypes being developed within the RD53 Collaboration [21].

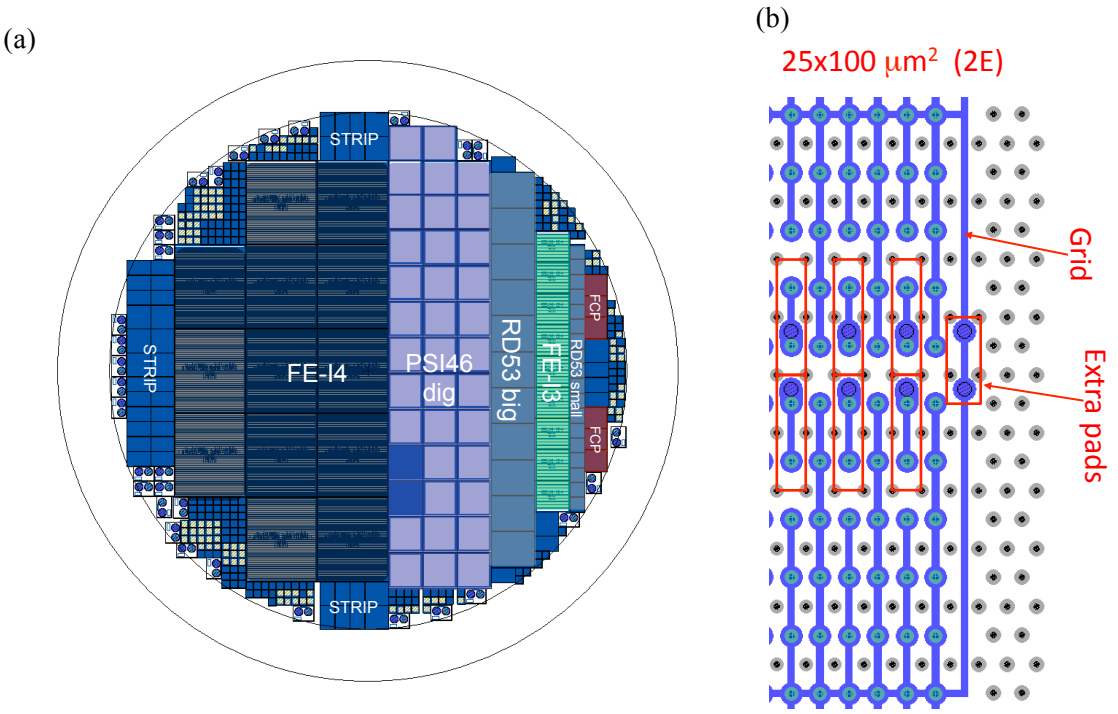

Figure 3 (a) Wafer layout of the first small pitch 3D sensors fabricated at FBK, and (b) layout details of 3D pixel sensors featuring 25×100 μm² cells size compatible with ATLAS FE-I4 read-out chip.

One major design issue was to make small pitch 3D pixels compatible with existing ROCs which feature larger native pixels, e.g., 50×250 μm² (FE-I4) and 150×100 μm² (PSI46dig). To this purpose, 3D elementary cells like those of Fig. 2 were placed on a regular grid of the desired small pitch size; one or more cells were then connected to the ROC bonding pads, whereas the remaining read-out columns were all shorted by a metal grid and connected to

the extra bonding pads (normally used for guard rings) that are grounded in the ROC (see Fig. 3b). Using such interconnection scheme, as many small pitch pixels as possible can be tested while ensuring proper boundary conditions, since all columns are uniformly biased, and keeping the ROC tuning simple, since all read-out channels have the same input capacitance. However, it should be noted that most of the sensor volume is not active, so that data analysis is more difficult due to incomplete clusters.

The periphery of the wafer layout hosts several smaller sensors (3D strips, 3D diodes) and test structures, aimed at easing the characterization without need of bump bonding. In particular, 3D diodes (~2 mm^2 area) reproduce the 3D elementary cells of the different pixel and strip sensors, but have all read-out columns shorted by a metal grid [6]. Owing to their small size, 3D diodes are often free from process-related defects, making it possible to investigate the intrinsic features of the technology and of the different designs.

From the electrical characterization of small pitch 3D diodes [22], the following observations were made: (i) the depletion voltage is very small, of the order of 2 - 3 V depending on the layout; (ii) the capacitance is ~50 fF per column; (iii) the leakage current is small, a few pA per column; (iv) the intrinsic breakdown voltage is higher than 150 V, with only a small fraction of devices showing lower values due to defects. All these results are very encouraging and in good agreement with TCAD simulation predictions (see Fig. 4), a part from the slope of the I-V curves. In fact, simulations fail in reproducing this feature because surface generation is not activated; moreover, since the simulation domain is an elementary 3D cell, it does not account for the increase with voltage of the depleted volume into the slim edge region.

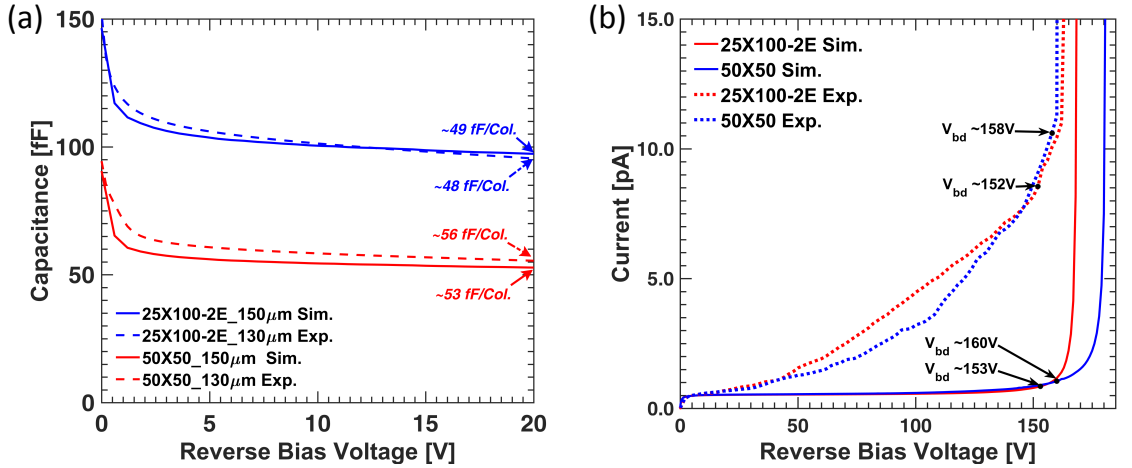

Figure 4 Simulated (solid lines) and measured (dashed/dotted lines) electrical characteristics of small pitch 3D pixels of 25×100 μm^2 (2E) and 50×50 μm^2 type from a wafer with 130 μm active thickness: (a) C-V curves, (b) I-V curves.

The I-V curves of all pixel sensors were measured on wafer with an automatic probe station making use of a temporary metal layer [6]. Compared to small 3D diodes, a larger incidence of process defects causing an early breakdown was observed in large area pixel sensors. However, considering this is the very first batch, the yield is high enough (>80%) on sensors compatible with PSI46dig (~1 cm^2), and still satisfactory (~38%) on sensors compatible

with FE-I4 (~4 cm^2). The best wafers in terms of leakage current and breakdown voltage have been selected for bump bonding to be performed at Leonardo SpA (Rome, Italy - former Selex SI) and IZM (Berlin, Germany). After bump-bonding, the first prototype modules were assembled at INFN Genova and characterized using 120 GeV pions at CERN SPS H6A beam line in August and October 2016, data analysis is under way.

In parallel, selected test structures were functionally tested in laboratory, starting with measurements with a position resolved infrared laser system (wavelength 1055 nm, pulse duration 40 ps, beam size 5 μm). Strip sensors of different elementary cell sizes were tested using an in-house made read-out board based on discrete components (charge amplifier + shaping filter with 100 ns shaping time). As an example, Fig. 5a shows a detail of the strip sensor layout of 50×50 μm^2 elementary cell size, including the region of interest for the laser scan. Only the first three strips closest to slim edge of the sensor are biased and read-out, whereas the rest of the strips are floating. Figure 5b shows the map of the signals measured at three different voltages (2, 8, and 50 V). The strip themselves are easily recognized in the signal map as the low signal regions at the center, due to the light reflection from the metal lines (note that the observed misalignment of the columns in the Y direction is due to a problem with the motorized translation stage, which missed some steps). It can be seen that high signal efficiency is achieved already at 2 V in the region in between the three biased strips, in good agreement with the depletion voltage value. In comparison, at the sides, the regions of high signal increase their sizes as the voltage is increased. As for the region on the right side of Fig. 5b, this is explained by the fact that strip #4 is floating, so that strip # 3 can collect charge from an active volume increasing its size with voltage. Similarly, for the region on the left side of Fig. 5b, this is due to the lateral extension of the depletion region of strip #1 within slim edge region, whose size increases with voltage. The extension of such depletion region at 50 V is about 70 μm, in very good agreement with the simulated value [17]. This confirms that the slim edge termination based on the ohmic column fence is effective and it allows for a very small dead area at the periphery (a few tens of μm).

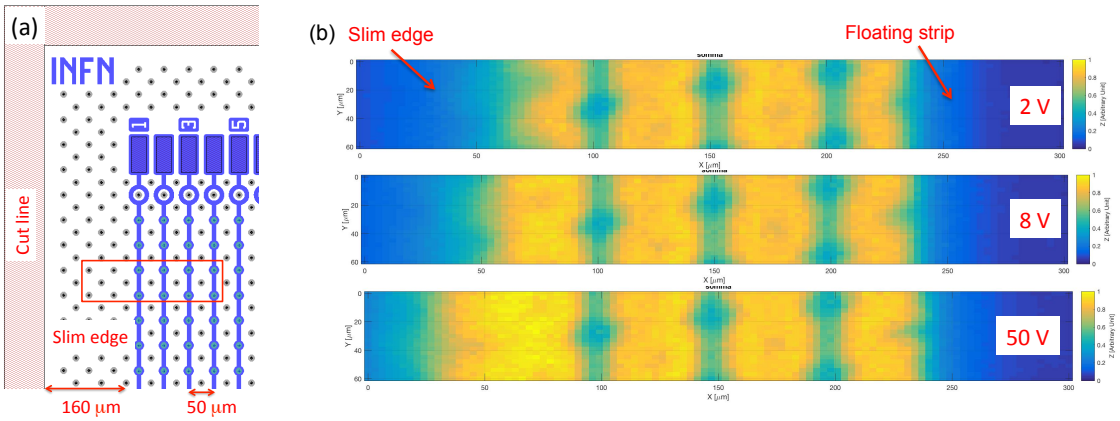

Figure 5 (a) Layout detail of 3D strip sensor of 50×50 μm^2 elementary cell layout (the red rectangle indicates the region of interest for the laser scan), and (b) maps of measured signals at three different bias voltage (2, 8, and 50 V).

An irradiation campaign of 3D diodes and 3D strips has been started, including X-rays (to investigate surface effects), neutrons, and protons. Devices will be tested in collaboration with the University of Freiburg (Germany) and the University of New Mexico (USA). In parallel, the design of a new batch of sensors oriented to devices compatible with the RD53A read-out chip [21] is under way, and is due by the end of the year to start production at FBK in January 2017.

4.2 Other on going projects: CNM and SINTEF

As mentioned in Section 3, CNM has also started to develop small pitch 3D sensors. This activity has been carried out within the CERN RD50 Collaboration, jointly with IFAE (Barcelona, Spain). A first batch fabricated with an improved double-sided technology was completed in 2015, including several pixel sensors compatible with existing ROCs [23]. The most significant results were so far achieved in a beam test, showing a hit efficiency of about 97% with orthogonally incident particles (compatible with the dead volumes due to columns) and up to 99.9% in case of 14° tilt. Remarkably, this was obtained at just 2 V bias before irradiation, in agreement with the very low depletion voltage. Further tests on irradiated devices are under way. Using the same wafer layout, CNM is processing a batch of small pitch sensors with a single-sided technology on SOI wafers of 70-150 μm active thicknesses. Moreover, another batch of double-sided 3D's with a layout dedicated to the RD53A ROC has also been launched.

SINTEF has also continued working at 3D sensor development, in collaboration with the Universities of Oslo and Bergen (Norway). The fabrication yield problems affecting the IBL qualification batches were understood, and FE-I4 pixel assemblies have been characterized in a beam test showing comparable performance to the FBK and CNM IBL modules [1]. Tests on irradiated samples are under way. Moreover, a new batch of sensors, including standard pitch and small pitch (RD53A compatible) devices, has been launched using both Si-Si DWB and SOI wafers of 50 and 100 μm active thickness.

5. Conclusions

3D sensor technology has made an impressive progress in the past few years: learning from the ATLAS IBL experience, a new generation of 3D pixel sensors is currently being developed for HL-LHC upgrades. In spite of the significant dimensional downscaling (about a factor of two), the fabrication of small pitch 3D sensors is feasible. Preliminary results from the first prototypes, both double-sided 3D's fabricated at CNM and single-sided 3D's fabricated at FBK, are very encouraging, with good electrical characteristics and high efficiency at low voltage before irradiation. Tests of sensors irradiated to large fluences are under way. New runs oriented to RD53A chip are being processed at different foundries and will be available in 2017.

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