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Design of analog front-ends for the RD53 demonstrator chip

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The RD53 collaboration is developing a large scale pixel front-end chip, which will be a tool to evaluate the performance of 65 nm CMOS technology in view of its application to the readout of the innermost detector layers of ATLAS and CMS at the HL-LHC. Experimental results of the characterization of small prototypes will be discussed in the frame of the design work that is currently leading to the development of the large scale demonstrator chip RD53A to be submitted in early 2017. The paper is focused on the analog processors developed in the framework of the RD53 collaboration, including three time over threshold front-ends, designed by INFN Torino and Pavia, University of Bergamo and LBNL and a zero dead time front-end based on flash ADC designed by a joint collaboration between the Fermilab and INFN. The paper will also discuss the radiation tolerance features of the front-end channels, which were exposed to up to 800 Mrad of total ionizing dose to reproduce the system operation in the actual experiment.

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1. Introduction

Unprecedented levels of radiation and particle rates will be reached in the future experiment upgrades at the Large Hadron Collider (LHC). With a peak luminosity of 5×10^{34} cm^{-2}s^{-1} and an expected average of 140 collisions per bunch-crossing, the High-Luminosity (HL) LHC will be delivering 3000 fb^{-1} of data after several years of operation, resulting in a set of challenging requirements for the detectors nearest to collision region, their sensor and readout chip. The front-end circuits will have to ensure reliable operation in a harsh radiation environment, with a predicted total ionizing dose of 1 Grad and a 1 MeV neutron equivalent fluence of 2×10^{16}cm^{-2}accumulated during their lifetime. Target pixel size for such experiments will be 50 μm $\times$ 50 μm for the inner-most layer of the tracker, with a power budget close to 0.5 W/cm^2, needed to minimize the material budget and the complexity of the cooling system, at hit rates in the order of 3 GHz/cm^2. With respect to current hybrid pixel detectors, featuring a typical sensor substrate thickness of 300 μm, thinner sensing device are being proposed for the Phase II upgrades. This will lead to smaller signals, exacerbating the requirements on the noise performance of the analog front-end electronics. In order to preserve the detection efficiency, operation of the readout channel at relatively small thresholds, around 1000 electrons or lower, has to be envisaged, setting challenging requirements on the equivalent noise charge (ENC) and the threshold dispersion.
The design of a new pixel readout chip complying with the tough specifications set by the aforementioned experiments upgrade is being tackled in the framework of the RD53 collaboration [1],[2] using a 65 nm CMOS technology. This technology node, whose radiation damage, due to both total dose and single event effects, has been investigated by the RD53 radiation working group, allows the designer to integrate the very dense in-pixel digital functions needed to comply with the bandwidth requirements set by the high rates foreseen in the experiments. The choice of this technology also allows for lower power consumption designs compared to technologies used in current projects (mainly 250 nm and 130 nm). It is a mature technology, being first introduced in the market in 2007, and it will be available for the foreseeable future, as it is widely used in the semiconductor industry.

2. Towards the RD53 full scale chip

The RD53 collaboration has been established with the aim of developing pixel readout integrated circuits for extreme hit rates and radiation levels. Around 20 institutions are involved in the collaboration, which has the support of both ATLAS and CMS experiments. The main goals of the collaboration include the detailed understanding of radiation effects in the 65 nm technology, the development of tools and methodology to efficiently design large complex mixed signal chips and, finally, the design and the characterization of a full sized readout chip featuring a 400$\times$400 pixel array with 50 μm pitch. A large scale chip, called RD53A, will be fabricated on an engineering wafer run shared with the CMS MPA chip [3] and other projects, and will include 400$\times$192 pixels with 50 μm pitch. This chip is not intended to be a final production IC for use by the experiments, and will contain design options for testing purposes, making the pixel matrix non-uniform. In particular, different versions of the analog front-end will be integrated in the RD53A, which will be submitted in early 2017.

2.1 65 nm prototype chips

Small demonstrators and test structure chips have been developed in the framework of the RD53 collaboration. In 2014, the INFN CHIPIX65 project submitted a set of prototypes including IP blocks and small matrices of pixels designed to the study of two different, one synchronous and one asynchronous, analog front end architectures [4]. The prototypes, intended to be radiation tolerant up to 500 Mrad total ionizing dose, have been submitted in October 2014 as three different 2×2 mm^2 chips to the foundry and have been characterized by the INFN groups involved in the CHIPIX65 project. The prototype integrating the front-end analog chains, called CHIPIX-VFE-1, includes an 8×8 pixel array with analog output featuring the synchronous architecture, and two 16×8 matrices with synchronous and asynchronous front-ends. It also includes standalone test structures for part of the analog chain, namely the charge sensitive amplifier and the threshold discriminator. A second prototype, called CHIPIX-VFE-2, has been submitted in 2015. It contains the same front-end architectures integrated in the previous one, with optimizations in some key points (in particular related to the threshold dispersion performance of the synchronous front-end), as discussed in [5]. These two versions of the analog front-end converged in the CHIPIX65 demonstrator, submitted in June 2016. Another design based on an asynchronous front-end, designed by the Lawrence Berkeley National Lab, is included in the FE65-P2 demonstrator. FE65-P2 aims at demonstrating very low, close to 500 electrons, stable threshold operations, that can be achieved thanks to excellent analog performance irrespective of the digital activity. Other goals are: the radiation hardness at least for 500 Mrad level and the design demonstration of the new concept of isolated analog front ends embedded in a flat digital design, referred to as "analog islands in a digital sea". The characterization of the structures included in the CHIPIX-VFE chips and FE65-P2 will be presented in section 3. A joint collaboration between the Fermilab and INFN led to the submission, in May 2016, of a 16×16 matrix including analog front-end with zero dead time and Flash ADC [6]. The characterization activity relevant to this front-end has started in October 2016 and will not be discussed in this work.

2.2 FE65-P2 and CHIPIX65 demonstrators

FE65-P2 and CHIPIX65 are small scale demonstrators that contributed to the design effort led by the RD53 consortium with the development of several building blocks, including different solutions for the analog front-end channel to be bump-bonded to the pixel sensor. They can be

Table 1: Main features of the FE65-P2 and CHIPIX65 demonstrators

	FE65-P2	CHIPIX65
Array size	64×64	64×64
Dimensions	3.5mm×4.2mm	3.5mm×5.1mm
AFE architecture	Single AFE	Multiple AFE
Digitization	4-bit ToT	5-bit ToT
In-time threshold	<1000 e-	<1200 e-
ENC	∼60e- @ C_D=100 fF	∼100e- @ C_D=50 fF
AFE current consumption	$\sim 4\ \mu$A	$\sim 4\ \mu$A

considered as a full exercise of chip integration and constitute a trial version before moving to the RD53A demonstrator. They both include a 64×64 pixel array with 50μm×50μm bump pattern, featuring the so called "analog island" arrangement, first introduced in the FE65-P2, where a cluster of four pixels, featuring horizontal and vertical symmetry, constitutes a regular structure where the analog part is completely surrounded by the digital logic. The FE65-P2 chip features a single analog front-end (AFE) architecture and is divided into eight regions including eight columns each for testing analog variants such as leakage current compensation and increased PMOS gate channel width for higher radiation tolerance [7]. The FE65-P2 analog front-end features an equivalent noise charge close to 60 electrons for a detector capacitance C_D=100 fF, with an in-time threshold smaller than 1000 electrons, while consuming a current close to 4 μA. A 4-bit Time-over-Threshold (ToT) counting is exploited for analog to digital conversion. The CHIPIX65 demonstrator integrates two different analog front-end architectures interfacing with a common digital readout and configuration scheme. One half of the pixel array is based on the synchronous operation of a comparator with offset cancellation, while the second one implements a completely asynchronous processing of the signals from the detector. These architectures are the ones validated through the aforementioned CHIPIX-VFE prototypes. Different silicon-proven IP blocks designed by INFN for RD53, such as biasing DACs, a bandgap voltage reference, a monitoring ADC, a high-speed serializer and custom SLVS drivers, have been also included. Both the analog front-ends integrated in the CHIPIX65 feature an ENC close to 100 electrons at 50 fF input capacitance, and take advantage of a 5-bit in-pixel ToT counter for signal digitization. The in-time threshold for both the architecture is smaller than 1200 electrons, with a static analog current consumption close to 4 μA [8]. The main features of FE65-P2 and CHIPIX65 are gathered in Table 1. As already mentioned, RD53A will be a multiple AFE chip adopting some of the solutions already implemented in FE65-P2 and CHIPIX65.

Concerning the isolation strategy between the analog and the digital parts of the chip, the solution integrated in the FE65-P2 relies upon the usage of two different deep N-wells, one for the analog section and one for the digital. In CHIPIX65 just the analog circuits are integrated in dedicated deep N-wells, while the digital section is laid out in the global substrate of the chip. The solution adopted in the RD53A is the same used in the FE65-P2 and just the PAD's ESD protection circuitry will be integrated in the global substrate. As far as the bias distribution is concerned, RD53A features a double stage mirroring scheme, already implemented in the CHIPIX65 demonstrator, where the currents generated in the matrix periphery by means of global DACs are first mirrored into biasing blocks integrated at the matrix column base and then mirrored to the column pixels. A single-stage mirroring scheme is instead implemented in the FE65-P2. On-chip bias monitoring capabilities have been also included into the CHIPIX65 demonstrator [8] and will be implemented in the RD53A as well.

3. Analog front-ends

Four different analog front-ends have been developed in the framework of the RD53. They are named as BGPV (stands for University of Bergamo and INFN Pavia), LBNL (Lawrence Berkeley National Lab), TO (INFN Torino) and FNAL (Fermilab and INFN Pavia). Three of them, namely BGPV, LBNL and TO, implement a time-over-threshold method to perform analog to digital con-

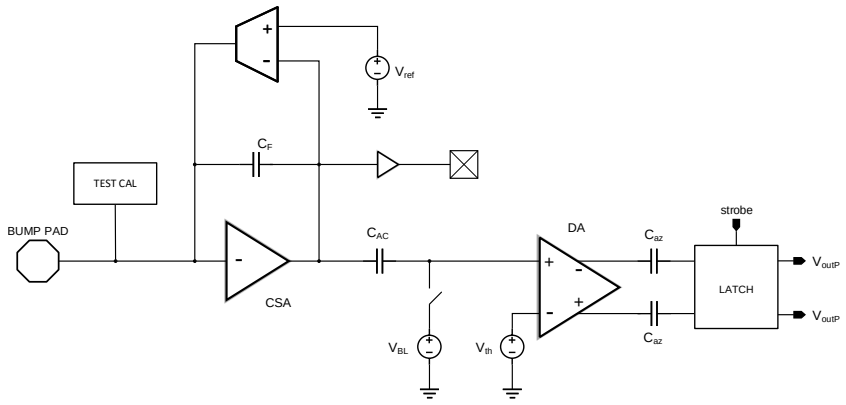

Figure 1: TO analog front-end chain.

version, whereas the FNAL readout chain is a zero dead time front-end based on flash ADC. Only the ToT-based front-ends will be integrated in the RD53A large scale chip.

3.1 TO front-end

The pixel analog chain designed by INFN Torino [9] is shown in figure 1. It implements a single stage charge sensitive amplifier (CSA) with a Krummenacher feedback network [10] providing both the feedback capacitor constant current discharge and the sensor leakage current compensation. The charge preamplifier is AC coupled to a synchronous discriminator composed of a differential amplifier (DA) and a positive feedback latch. A telescopic cascode architecture has been envisioned for the the CSA forward gain stage featuring a DC open loop gain close to 60 dB. Due to mismatch effects, considerably relevant in deep submicron technologies like 65 nm, the CSA output baseline is subject to quite large fluctuations (of the order of tens of mV) between different channels. This led to the AC coupling of the preamplifier to the discriminator DA. In this design an offset compensation using internal capacitors has been chosen. A compensation phase lasting around 100 ns every 100 μs is required. This choice allows doing a local threshold trimming, without the need of a correction DAC. The discriminator output fed to the ToT counter for digitization is generated by the positive feedback latch stage, directly connected to the differential output of the DA. The latch stage has been designed to minimize mismatch effects causing a dynamic offset contributing to the overall threshold dispersion. The latch can be turned into a local oscillator up to 800MHz by means of an asynchronous logic feedback loop in order to internally generate a clock that can be used for high-speed ToT digitization. The total current consumption of the front-end, including the latch, is close to 5.5 μA. The contribution of the analog blocks, namely the CSA and the DA, is close to 3.5 μA. Threshold dispersion measurements have been carried out on the front-ends integrated in the CHIPIX-VFE1 and CHIPIX-VFE2 chips. In the first prototype the threshold dispersion with the offset compensation, measured on a set of 16 pixels, is close to 174 electrons. This data has to be compared with the uncompensated front-end, featuring a dispersion of 273 electrons. Actually, the decrease in the dispersion introduced by the offset compensation is smaller than expected. This led to the optimized front-end version integrated in CHIPIX-VFE2, featuring a threshold dispersion close to 70 electrons. Such a prototype chip has been irradiated up to

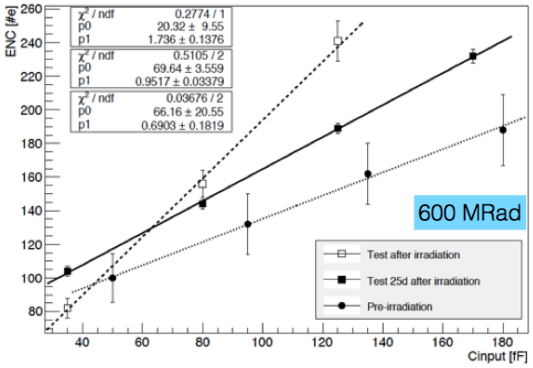

Figure 2: ENC as a function of the CSA input capacitance for the TO analog front-end.

600 Mrad of total ionizing dose (TID) at CERN X-ray machine. The chip was biased, clocked and the readout kept active during the irradiation. Measurement results show that the front-end is still fully working at 600 Mrad, with negligible degradation of the analog parameters. As an example, Fig. 2 shows the equivalent noise charge as a function of the capacitance shunting the CSA input. A 10% noise increase has been detected for a capacitance of 50 fF, which is the expected value for the detector capacitance. A 25% increase in the preamplifier peaking time has been measured, with a partial recovery with annealing at room temperature. Also the ToT frequency is affected by radiation, decreasing with the TID and, again, a partial recovery after annealing. A recovery after annealing is detected also for the ENC [11].

3.2 BGPV front-end

The asynchronous analog front-end designed by University of Bergamo and INFN Pavia [12] is shown in figure 3. The readout chain includes a charge sensitive amplifier featuring a Krummenacher [10] feedback complying with the expected large radiation induced increase in the detector leakage current. The choice of a single amplification stage in the front-end channel has been simply dictated by power consumption and area constraints. The signal from the CSA is fed to a

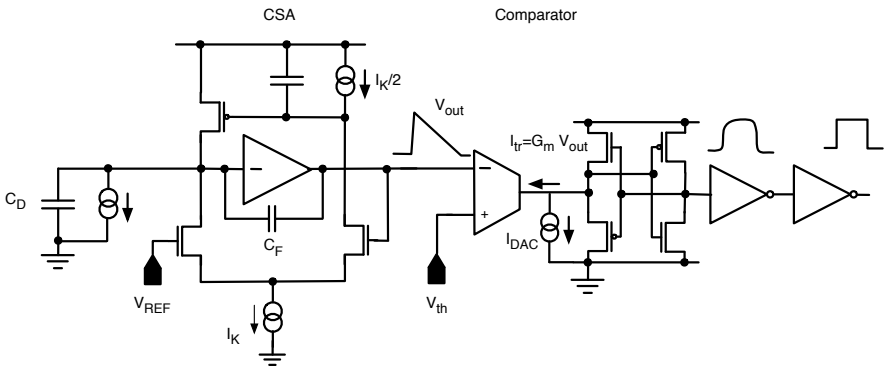

Figure 3: Asynchronous analog front-end chain designed by University of Bergamo and INFN Pavia.

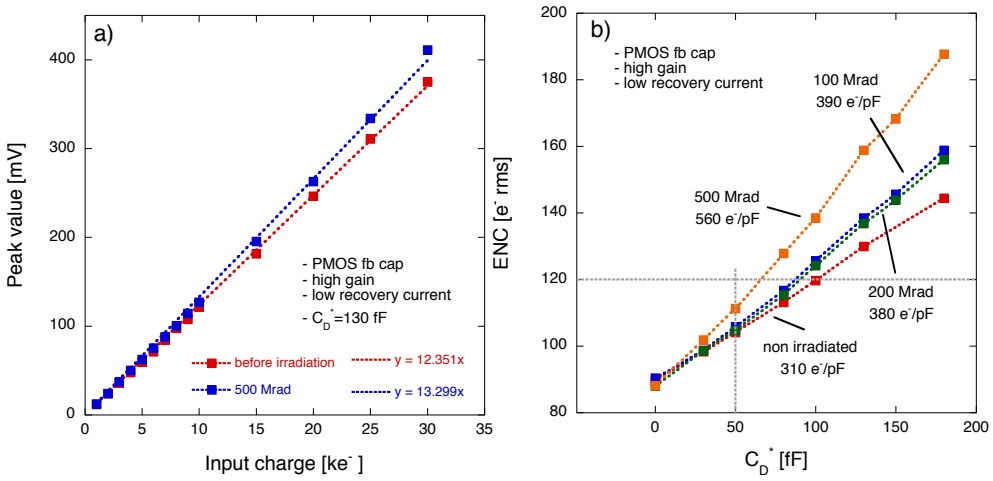

Figure 4: a) Peak response of the charge preamplifier as a function of the input charge for the fresh device and for the device irradiated at 500 Mrad. b) Equivalent noise charge as a function of the total CSA input capacitance for the non-irradiated device and for the front-end irradiated at different doses. The CSA feedback capacitance is implemented with a PMOS device.

high-speed, low power current comparator [13] that, combined with a 5-bit, dual edge time-over-threshold (ToT) counter, is exploited for time-to-digital conversion. Channel to channel dispersion of the threshold voltage is addressed by means of a local circuit for threshold adjustment, based on a 4-bit binary weighted DAC generating the current I_{DAC}. The front-end chain is optimized for a maximum input charge equal to 30000 electrons and features an overall current consumption close to 4 μA. The forward gain stage of the charge sensitive amplifier features a folded cascode architecture including two local feedback networks boosting the signal resistance seen at its output node. With a current flowing in the input branch equal to 3 μA and a current in the cascode branch close to 200 nA, the CSA is responsible for most of the power consumption in the analog front-end. The DC gain and the -3dB cutoff frequency of the open loop response, as obtained from simulations, are 76 dB and 140 kHz respectively. The front-end channel includes a high-speed, low power threshold discriminator, based on current comparison, connected at the preamplifier output. It includes a transconductance stage whose output current is fed to the input of a transimpedance amplifier providing a low impedance path for fast switching. The threshold dispersion after tuning, obtained from circuit simulations with the Spectre simulator, is close to 35 electrons, thanks to a correction factor close to 10 introduced by the 4-bit, in-pixel trimming DAC. Two separate irradiation campaigns have been carried out for this front-end. In the first one the samples have been irradiated up to 800 Mrad as bare dice with no bias applied. During the second one, the samples, irradiated at a dose up to 500 Mrad, were mounted on a PCB and biased as in operation. Very small changes were detected in the charge sensitivity, as shown in Fig. 4 a), and in the shape of the signal at the preamplifier output, even at the highest dose. As far as the noise is concerned, a 10% increase in the ENC for a CSA input capacitance (C_D^* in Fig. 4 b)) of 50 fF has been detected at 500 Mrad TID which nevertheless remain compliant with the demanding HL-LHC experiment specifications. The ENC slope goes from 310 e-/pF in the non-irradiated device to 560 e-/pF in DUTs exposed

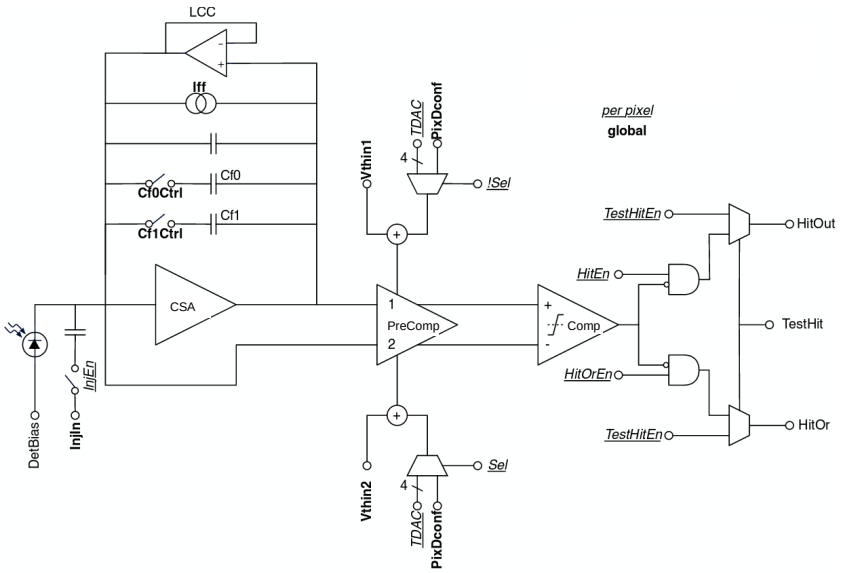

Figure 5: Analog front-end chain designed by LBNL.

to a total ionizing dose of 500 Mrad. The ENC increase is likely related to degradation in the low frequency noise of the preamplifier input device. A comprehensive discussion concerning radiation tolerance for this front-end can be found in [14].

3.3 LBNL front-end

The analog front-end designed by LBNL, included in the FE65-P2 demonstrator, is a continuous-time analog processing channel schematically shown in Fig. 5. It is based on a 2-stage comparator and a charge sensitive amplifier whose input is used as a reference for the comparator's first stage, referred to as the pre-comparator. The analog to digital conversion is implemented entirely in the digital core, by digitizing the time-over-threshold of the comparator output pulse. The CSA is

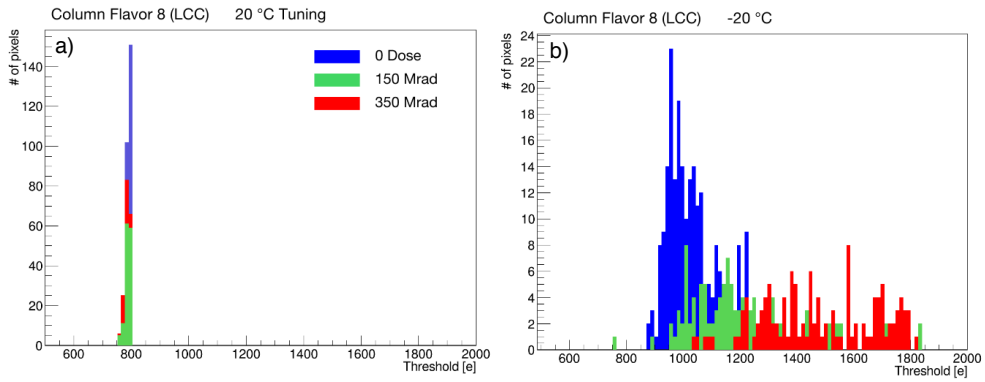

Figure 6: a) Threshold distributions for the fresh device and for the chips irradiated at 150 and 350 Mrad. Chips were tuned at 20°C to 800 electrons. b) Threshold distributions of the samples at -20°C.

based on a simple straight regulated cascode architecture with NMOS input transistor operating in weak inversion. It features a current mirror constant current feedback and the gain can be adjusted by choosing between four possible values of feedback capacitance. The value of the current discharging such a capacitance can be set globally and cannot be trimmed at pixel-level. Nevertheless, an acceptable value of the dispersion of the return time to the baseline, directly related to the ToT dispersion, has been obtained from prototype measurements. For leakage currents below 10 nA, the continuous feedback is capable of preventing the input from saturating. On the other hand, for larger currents, a leakage current compensation circuit has to be envisaged, as shown in Fig. 5. The first stage of the comparator, DC-coupled to the preamplifier, provides additional gain and acts as a differential threshold circuit. Global threshold DACs in the matrix periphery provides the Vthin1 and Vthin2 bias generating effective differential supplies for the pre-comparator. Local tuning of the threshold is performed by exploiting one 4-bit resistor ladder in each pre-comparator branch. The pre-comparator stage is followed by a classic continuous time comparator stage with output connected to the digital pixel region through logic gates. The pseudo-differential design reduces variation due to mismatch and provides improved power supply rejection. Early results with bare chips pointed out excellent analog performance in term of noise and threshold dispersion. In particular, an equivalent noise charge close to 35 electrons has been measured for a detector capacitance of 50 fF, with threshold dispersion after tuning close to 40 electrons and a current consumption close to 4 μA. The value of the ENC is close to 60 electrons when the front-end is set up in such a way to meet the RD53A specifications.

Uniform and stable response of all pixels is a critical requirement for pixel detector operation. Gradual threshold drift can be compensated by means of periodic tuning, which is only feasible in long enough gaps between data runs. A pixel chip design must therefore be robust against changes in temperature and radiation dose in order for the response to remain stable during at least one run. For this reason, the threshold evolution with the radiation and the temperature has been investigated for this design. In particular, the rates of shift for threshold mean and dispersion have been assessed for chip irradiated at 150 and 350 Mrad. With respect to the fresh device, the shift in mean is smaller for the sample irradiated at 150Mrad. The rate of dispersion due to early dose is in the range of 100 e-/Mrad for the fresh device, while rates of the order of 10 e-/Mrad have been obtained for the devices irradiated at 150 and 350 Mrad. The behavior of the threshold with the temperature has been evaluated as well. As an example, Fig. 6a) shows the threshold distributions relevant to one flavor of the AFEs integrated in the FE65-P2 (in particular the one including the leakage current compensation circuit) just after tuning at 20°C, for the fresh device and for the irradiated samples. Fig. 6b) shows the distribution of each chip at -20°C without retuning. Both the mean value of the threshold and its dispersion increase with decreasing temperature, and the magnitude of the effect scales with total radiation dose. A comprehensive discussion can be found in [7].

3.4 FNAL front-end

A synchronous analog processor with zero dead time, named iFCP65, has been designed in a 65 nm CMOS technology by a joint collaboration between the Fermilab and INFN. It includes a low noise, fast charge sensitive amplifier with detector leakage compensation, and a compact, single ended auto-zeroed comparator featuring very good performance in terms of channel-to-channel

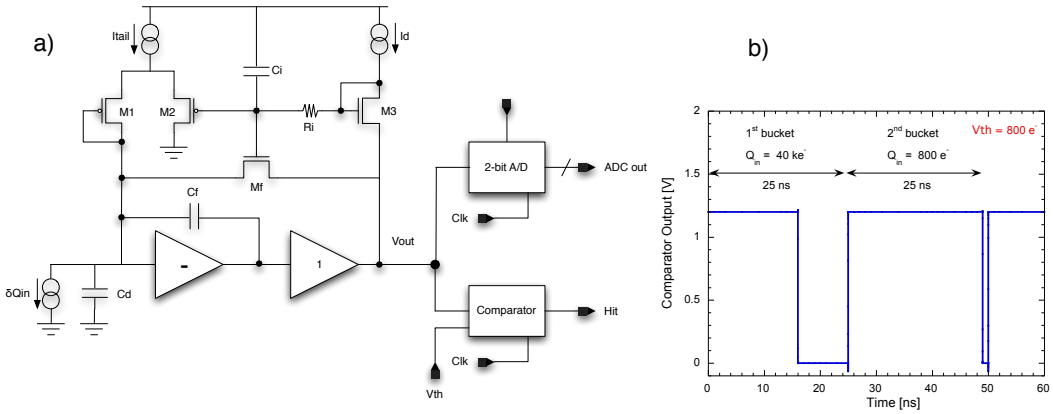

Figure 7: a) Zero dead time front-end designed by Fermilab/INFN Pavia. b) Comparator output response to two consecutive events (40000 and 800 electrons) with a threshold set to 800 electrons.

threshold dispersion. The schematic diagram of the analog processor is shown in Fig. 7a). The first stage of the processing chain is a charge sensitive amplifier, featuring a current consumption of 4 μA and implementing a regulated cascode scheme in its forward gain stage. It also includes a source follower stage able to properly drive the CSA load. The charge amplifier features a feedback leakage compensation network able to cope with leakage currents up to 15 nA. Notice that the expected leakage current will remain at or below 10 nA per pixel at operating temperature after radiation damage. These characteristics seem achievable with both planar and 3D sensors of thickness in the range 100 to 150 μm and with pixel area of 2500 mm^2. The signal at the CSA output is fed to a compact, single-ended threshold discriminator with auto-zeroing features providing a pure hit/no-hit information at the channel output. The current consumption for this stage is close to 1 μA. Compared to a typical implementation of the discriminator, where voltage comparison takes place exploiting a differential MOS pair with a mirrored load, the circuit implementation used in this readout channel is ideally insensitive to device threshold voltage mismatch. For this reason, the comparator, run with a 40 MHz clock, does not require any threshold fine-tuning system. A 2-bit flash ADC, whose architecture is based on the same circuit used for the hit comparator, is exploited for digital conversion immediately after the charge sensitive amplifier. A peculiar feature of the iFCP65 comparator is its capability to process signals belonging to two consecutive bunch crossings. As an example, Fig. 7b) shows the simulated comparator output response to two consecutive charge signals injected into the readout channel. Simulation has been carried out with the Spectre simulator. In this simulation the comparator clock is set to 40 MHz, and the threshold to 800 electrons. In the first bucket, lasting 25 ns, the comparator responds to a charge signal equal to 40000 electrons injected at the CSA input, whereas in the second one it responds to a charge equal to 800 electrons. This points out that the iFCP65 readout channel is able to successfully process very large signals followed by signals close to the threshold.

4. Conclusion

Future pixel detectors at the High-Luminosity LHC require a new generation of readout chip

complying with severe requirements in terms of speed, noise, power consumption and radiation hardness. Four different analog front-ends flavors have been developed in the framework of the RD53 collaboration.The main analog performance have been assessed for each analog front-end. Very good noise performance have been obtained from experimental results, with an equivalent noise charge close to 35 electrons for the LBNL front-end and ENC close to 100 electrons for the other front-ends. Very good results have been obtained also in terms of threshold uniformity, with a threshold dispersion ranging from 35 electrons (LBNL front-end) to 70 electrons (TO front-end). The threshold evolution with the radiation and the temperature has been investigated for the LBNL design. The FNAL front-end features a zero dead time processor including a comparator able to correctly process signals in consecutive bunch crossing periods. The RD53 collaboration is currently working on the design of a large scale demonstrator, RD53A, which will be submitted in a 65 nm technology in early 2017. One of the main goal of such a chip is to demonstrate the feasibility of the 65 nm technology in facing the challenging requirements set by the future experiment upgrades.

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