PROCEEDINGS OF SCIENCE

Development of detector technologies for ILC vertexing

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The physics programme at the ILC relies heavily on pure and efficient identification of heavy-flavour quarks, requiring pixel vertex detectors with 3–4 μm hit resolution and a material budget of 0.1–0.2% of a radiation length per layer.

Although technology choices are still several years in the future, a number of detector concepts are currently being actively studied. I will discuss these concepts and the associated ongoing R&D programmes, including potential sensor technologies (CMOS, CCD, DepFet etc) as well as mechanical and system issues.

The 25th International workshop on vertex detectors
September 26-30, 2016
La Biodola, Isola d'Elba, ITALY

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PoS(Vertex 2016)050

1. Introduction

The design choices for vertex detectors at the proposed International Linear Collider [1] are dictated by the demanding physics requirements and background environment [2]. In particular the decays of heavy flavoured particles must be identified with high purity and efficiency through the measurement of tracks displaced from the nominal interaction vertex, in the presence of a high rate of background hits from low-energy e^+e^- beamstrahlung pairs.

To meet this challenge designs have converged on multi-layer silicon pixel detectors spanning the radii from just outside the beam pipe (approximately 14 mm) to about 60 mm. These designs typically have five concentric cylinders ("barrels") of detectors equally spaced in radius, or six layers of detectors arranged as three equally spaced double layers. Within each double layer a pair of detectors is supported on the same mechanical structure, separated in radius by 1–2 mm. The active length of the detector in z will be 25–30 cm, which could be a single long barrel region, or a short barrel with 2–3 disks added at each end to enhance measurements in the forward regions.

The required hit resolution is about 3 μm in both $r-\phi$ and z, but to reduce the effects of multiple scattering for low-momentum tracks the material in each layer must be kept to a minimum: 1–1.5% X_0 per layer. This precludes the presence of cooling elements within the active volume, so all designs assume that heat will be removed by flowing dry air or nitrogen through the detector. This, in turn, places severe restrictions on the power dissipated by the electronics. It is therefore envisaged that most (if not all) electronic power will utilise "power pulsing": switched on for a short time around the arrival of the 1 ms bunch train; switched off for most of the 199 ms between trains.

There is a large degree of uncertainty on the prediction of the rate of background hits. However, even in the most optimistic scenarios the density of hits produced over an entire bunch train will cause an unacceptably high occupancy and overwhelm the pattern recognition, particularly in the innermost layer. The two approaches being considered to tackle this are either to provide timing information within a bunch train, or to use very small pixels with novel pattern recognition techniques.

The contradictory technological challenges for an ILC vertex detector are therefore to provide extremely precise (and therefore stable) tracking with a minimum of material, possibly with microsecond (or faster) timing and a minimum of power dissipation. Here we will discuss a number of R&D efforts within the global ILC detector community that aim to meet these challenges. It must be noted, however, that final technology choices for the ILC vertex detectors will not have to be made for several years. It is therefore possible that developments made for other HEP projects (perhaps as described elsewhere in these proceedings), other fields, or even in industry may provide simple and cost effective solutions for the ILC.

2. DepFET

The DepFET collaboration have reported at this conference [3] on their latest developments. In a DepFET device, charge generated by the passage of an ionising particle through the sensitive layer within a pixel collects on the gate of a FET. The charge can then be detected by measuring

the current when the transistor is biased. Belle II is currently building a new DepFET-based vertex detector, but the technology has long been considered as a candidate for ILC vertex detectors.

Custom processing has been developed for DepFET sensors that allow all material other than the sensitive volume to be removed. ILC-targeted prototypes have been manufactured that are 50 μm thick in the pixel region, surrounded by a frame of un-thinned 300 μm thick silicon that provides mechanical stability. The material averaged over a layer (including driver and readout ASICS) is expected to be less than 0.1% X_0.

Devices with pixel sizes down to 24 μm$\times$24 μm have been studied in test beams, and the results have confirmed that the target spatial resolution should be achieved. Testing of power pulsing and air cooling has given confidence that the electronic performance and mechanical stability will be sufficient in the ILC environment. The DepFET collaboration has also successfully integrated microchannel cooling into its designs, which could offer a safety margin over pure gas flow cooling while adding only a minimum of material.

3. Monolithic CMOS

The development of CMOS imaging technology is proceeding rapidly due to commercial stimulus, and the technology is maturing within HEP. As with DepFETs, ILC-targeted R&D has found application within other HEP projects (STAR [4], EUDET/AIDA beam telescopes etc.) and developments within other programmes (e.g. HL-LHC) is starting to feed back to ILC R&D.

The STAR vertex detector has had a successful physics run using sensors in the Mimosa/-Ultimate/Mistral family, developed by the PICSEL group at IPHC Strasbourg. These utilise a 0.18 μm CMOS imaging process and are routinely thinned to 50 μm. The Mimosa-22 variant, a test device for the ALICE ITS [5], has demonstrated good performance even after radiation doses far greater than those which will be accumulated at the ILC.

The timing information required to reduce the ILC background occupancy can be achieved by distributing a timing signal and storing the time of each hit within a pixel during the bunch train. Unfortunately, it is believed that the current 0.18 μm CMOS technology will not be able to provide this functionality in pixels small enough to give the target spatial resolution. The proposed solution is to make two varieties of ILC sensors, one with high spatial resolution but no timing, and one with larger pixels with timing but worse spatial resolution. These sensor varieties would be placed together in double layers, separated by 2 mm in radius. After each bunch train, both layers would be read out and the hits correlated.

The principle of double layers for the ILC has been demonstrated by the PLUME collaboration [6]. Two modules, each consisting of six Mimosa-26 sensors mounted on a flex circuit, are attached to opposite sides of a 2 mm thick silicon carbide foam substrate to make a rigid double-sided "ladder". These devices have been tested in beams and the measured hit resolution was consistent with expectations. A new version of the PLUME design is currently being prototyped using aluminium flex circuits to help achieve a material budget of 0.35% X_0 per double layer, and a full programme of thermal and mechanical tests is planned.

A separate CMOS development is the Oregon/Yale Chronopix design [7], which hopes to achieve bunch time stamping with 3 μm spatial resolution by using a 90 nm process. The current

variant has a 25 μm×25 μm pixel, and various pixel and processing options have been tested to optimise the noise and eliminate cross talk.

4. Integrated Approaches

There are a number of approaches which integrate CMOS with other processes, such as Silicon-on-Insulator (SOI) technology. In SOI devices the layer of CMOS electronics is isolated from the charge-collection region, typically by bonding a CMOS wafer to a detector wafer which has an SiO_2 layer on the surface.

The SOFIST [8] project is developing an ILC pixel sensor with SOI technology. The functionality will be similar to the monolithic CMOS variants described above, with hit times stored in registers. The current test design incorporates an array of 2500 20 μm $\times$ 20 μm pixels, each with two registers to record bunch-by-bunch timing.

FNAL [9] developments have gone even further, with multi-layer "3D" integration. The VIP demonstrator is an ASIC with 24 μm $\times$ 24 μm pixels fabricated as separate analogue and digital layers that are bonded directly together. The VIP can then be fused to a third, sensor, silicon layer.

5. Fine Pixel CCDs

For pixel sizes of 5 μm $\times$ 5 μm the maximum occupancy over a bunch train is expected to be manageable at around 1%. Such small pixel size can be achieved using CCDs, and this is the logic behind the Fine Pixel CCD (FFPCCD) development [10]. CCDs are far more sensitive to radiation damage than CMOS devices due to charge trapping during transport, but FPCCD prototypes have shown acceptable charge transfer efficiencies after ILC-level radiation doses when operated at -40°C.

Although the fine pixels reduce the occupancy, background hits still need to be eliminated before pattern recognition is performed to find tracks. This will first be done by removing extended clusters in $r-\phi$, as these are consistent with low momentum tracks with a large curvature. Surviving clusters will then be matched between two closely-spaced layers to confirm they are from a single high momentum particle.

Prototype 2 mm-spaced double layer structures have been built with the CCDs mounted on flex circuits attached to a carbon fibre support structure. Investigations are underway into CO_2 cooling to achieve the low operating temperatures.

6. Beyond the Vertex Detector

As CMOS technology matures, increasing in functionality and decreasing in cost, it becomes a natural candidate for use in other parts of ILC detectors. R&D has been carried out into the use of CMOS pixel sensors as the active layer in electromagnetic calorimetry, and a CMOS tracker could be lower mass, lower cost and more robust than one made with silicon strip detectors.

An example of preliminary work in this area is the monolithic Cherwell [11] sensor, which utilises a deep p-well to shield the CMOS circuitry within each pixel, preventing the leakage of

signal charge into the n-doped regions. In addition, the analogue circuitry is a "4-T" design, standard in modern optical sensors but relatively new in particle physics, in which much improved noise performance is achieved by transferring the signal charge from the collection diode to a separate, lower-capacitance node before reading it out.

Four different pixel configurations are included in Cherwell, two optimised for digital calorimetry, and two with pixels ganged together to make short strips for tracking. In three variants (both calorimeter and one tracker configuration) the analogue charge is digitised in ADCs placed conventionally at the periphery of the chip. In the second tracking variant, however, the ADC circuitry is distributed across the sensitive area in additional p-wells within each pixel. Future monolithic sensors could use similar techniques to add functionality via complex CMOS circuitry with no loss in analogue performance, and no "dead" area at the edge of the device.

7. Next Steps

Although the ILC community is developing several potential technologies, no full-scale devices meeting all requirements have yet been demonstrated. Over the next few years, the R&D collaborations will have to work towards qualifying prototypes over the full range of ILC operating scenarios. Given the uncertain time-scales, however, there is opportunity for new technologies to enter the field of candidates, possibly taking advantage of the synergies with other projects.

8. Conclusion

There are number of active R&D collaborations pursuing pixel sensor technologies to meet the challenge of the ILC vertex detectors, including DepFET, monolithic CMOS, integrated CMOS and Fine Pixel CCDs, and there is also ongoing work on mechanical integration and cooling. These activities contribute to and benefit from synergies with other HEP experiments, as well as developments in industry. CMOS pixel sensors could also potentially be used in ILC tracking and calorimetry detectors.

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