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# A monolithic pixel sensor with fine space-time resolution based on silicon-on-insulator technology for the ILC vertex detector

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We have been developing a new monolithic pixel sensor with silicon-on-insulator (SOI) technology for the International Linear Collider (ILC) vertex detector system. The new SOI sensor SOFIST can store both the position and timing information of charged particles. We will implement small pixel circuit with $20\times20$ $\mu$m$^2$ to achieve 3 $\mu$m single point resolution. The beam collision of ILC occurs every 554 nsec during a bunch-train injection of 1 msec. The pixel also records the hit timing with an embedded time-stamp circuit to identify the hit event of each bunch collision. The sensor chip has column-parallel analog-to-digital conversion (ADC) circuits and zero-suppression logic for high-speed data readout. We are currently designing and evaluating two prototype sensor chips for optimizing and minimizing the SOFIST pixel circuit.

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*Speaker.





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## 1. Introduction

Silicon-on-insulator (SOI) wafer technology can be used to achieve a monolithic pixel detector [1], which integrates both a silicon sensor and readout electronics in the same wafer. The pixel sensor with the SOI technology has a multi-layer structure in which a CMOS circuit layer is bonded to a high-resistivity sensor layer. The buried oxide layer insulates these two layers. SOI pixel sensor has following advantages.

- Low material budget owing to the monolithic detector structure.
- Smaller pixels with non-mechanical bump-bonding.
- Implementation of complex functions in a pixel with a standard CMOS circuit process.

The SOI pixel sensor is suitable for the pixel sensor of the vertex detector in high energy physics experiments because of low material budget and good position resolution with small pixel. In addition, we are developing a pixel sensor with a double-SOI wafer (Figure 1). The additional layer of the double-SOI wafer can compensate the effect caused by the accumulation of holes in the oxide layer [2]. The double-SOI sensor has higher radiation tolerance for total ionization dose.

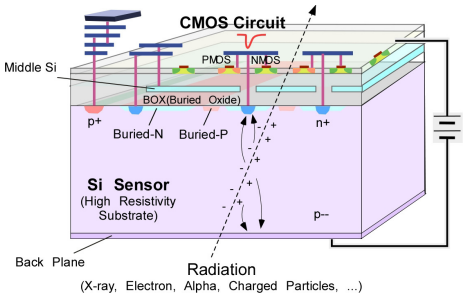


**Figure 1:** Structure of the double-SOI pixel sensor. A double-SOI wafer has an additional middle silicon layer in the middle of buried oxide layer.

We are studying the development of new SOI pixel sensor optimized for the vertex detector system of International linear collider (ILC). The physics goals at the ILC are the precise measurement of Higgs boson and the search for new physics beyond the Standard Model [3]. The ILC vertex detector system is required to be developed using a new pixel sensor with higher position resolution and finer time resolution. We are currently developing a new SOI pixel sensor, SOi sensor for FIne measurement of Space and Time (SOFIST).

In this paper, we report the development status of the prototype sensor chips for the SOFIST pixel circuit integration.

## 2. SOFIST overview: SOI pixel sensor optimized for ILC

We have the following target performances for the SOFIST development.

1. Single point resolution

We are designing a pixel circuit with a pitch less than 25 $\mu$m to achieve a detector vertex resolution of 5 $\mu$m. We improve the sensor position resolution by finding the hit position with centroid calculation from the signal charge spread among multi-pixels. The target of single point resolution is better than 3 $\mu$m. The vertex detector system also requires thinner sensors, less than 100 $\mu$m thick, for reducing the deviation of the particle trajectory by the multiple-scattering effect. The sensor wafer will be thinned to 50 $\mu$m.

2. Timing resolution

   The ILC beam has a bunch-train structure (Figure 2). The detector system accumulates event signals during the injection of one beam train. We need the timing resolution for the event separation during beam-bunch collisions. The sensor records the event timing by adopting an in-pixel time-stamp circuit.

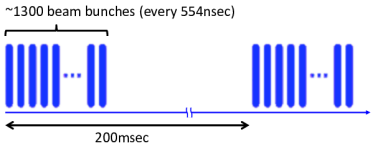


**Figure 2:** ILC beam train structure. One train consists of 1,300 bunches injected every 554 ns.

Figure 3 shows the sensor overview of the SOFIST. SOFIST has a pixel circuit with an area of 20×20 $\mu$m$^2$. The pixel signals are converted to digital data in parallel by the ADC circuit located at each pixel readout column. After digital data conversion, the zero-suppression logic circuit discriminates the signal data of hit pixels for reducing data transfer time.

SOFIST pixel circuit stores both the charge signal and the timing information of hit particles during one beam train. The sensor signal is input to in-pixel comparator. When the signal is over the threshold voltage, the hit signal amplitude and timing are both stored to each memory respectively. In order to accumulate multiple hits during the signal accumulation of one beam train, the pixel cell has more than two analog signal and time-stamp memories.

## 3. Development and Evaluation of prototype sensors

The steps of the prototype sensor development for evaluating the pixel circuit is as follows. We have already designed Ver.1 and Ver.2 prototype chips. The sensor chip is fabricated using 0.2 $\mu$m SOI process of the LAPIS Semiconductor.

- Ver.1: Pixel with analog signal readout and column ADC.
- Ver.2: Pixel with time-stamp and zero-suppression logic.
- Ver.3: Pixel that integrates both analog signal readout and time-stamp circuits.

### 3.1 Ver.1 sensor

Figure 4 shows Ver.1 prototype sensor chip. We adopted an N-type floating-zone (FZ) wafer with 2 k$\Omega$·cm in resistivity. This Ver.1 chip has the pixel circuit of 20×20 $\mu$m$^2$ and column-parallel

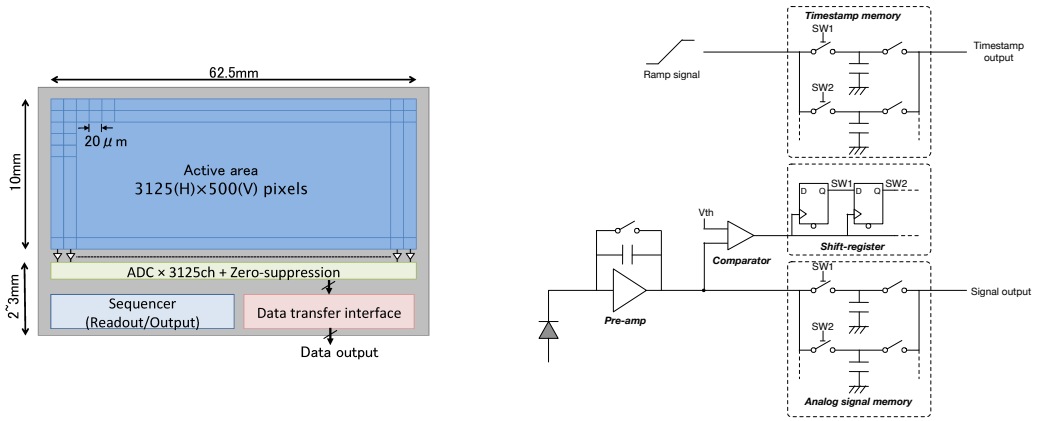


**Figure 3:** Schematic overview (left panel) and pixel architecture (right panel) of SOFIST. The sensor chip has 3,125×500 pixels. The column-parallel ADC and the digital circuits are arranged along the longitudinal direction of the sensor chip. The pixel circuit stores both the amplitude and timing of the input signal.

ADC circuits. The pixel circuit has the charge sensitive amplifier (CSA) with a common-source stage and a feedback capacitance. We designed the CSA circuit with feedback capacitances of 5fF with a conversion gain of 32 $\mu$V/e-. The CSA output signal is stored in the memory capacitor. This pixel has two analog memories for accumulating two hit signals. The pixel output signal is readout by on-chip column ADC circuits. We adopted Wilkinson-type ADC based on the circuit previously developed by SOI group [4]. The conversion time is approximately 10 $\mu$s per pixel line.

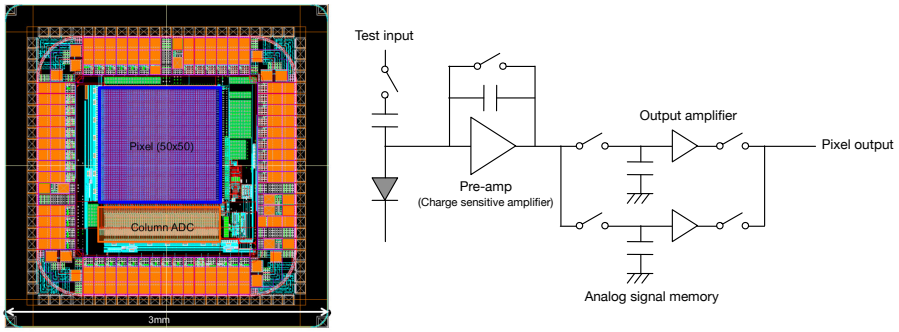


**Figure 4:** The chip overview (left panel) and pixel schematic (right panel) of SOFIST Ver.1.

The Ver.1 sensor chip has already been fabricated and being evaluated. We verified the analog signal readout of the pixel circuit and the function of column-ADC with $\beta$-ray irradiation. Figure 5 shows output signal image and spectrum of $\beta$-ray of Sr-90 radioactive check source. We reconstructed the spectrum with the signal clustering of multi-pixels. We can find a peak of $\beta$-ray from the cluster signal spectrum. The Ver.1 pixel and ADC has enough gain performance for detecting the signal of charged particle.

### 3.2 Ver.2 sensor

Figure 6 shows Ver.2 sensor chip. The Ver.2 pixel has a comparator circuit for discriminating the signal over the threshold voltage. A shift-register circuit is located at the output of the comparator. The shift-register switches the input of two analog memories. This pixel circuit also stores the

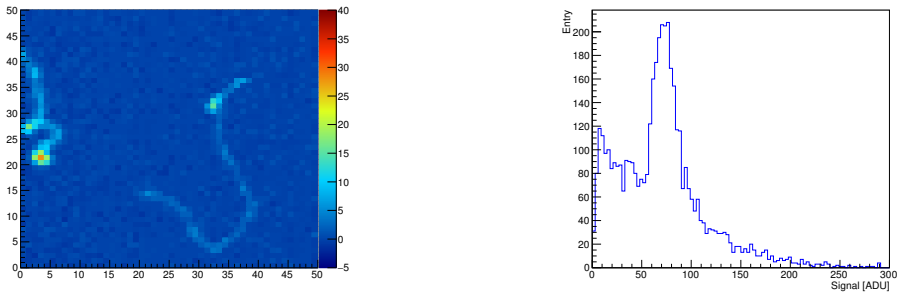


**Figure 5:** $\beta$-ray tracks and signal spectrum taken by Ver.1 sensor. These signal data were readout from on-chip column ADC.

hit signals of up to two events. We have designed two types of pixel circuits in Ver.2 chip, Analog signal pixel for storing the signal amplitude and Time-stamp pixel for analog time-stamp. A ramp waveform proportional to the elapsed time is input to the analog memories in the Time-stamp pixel. This analog time-stamp records the hit-timing information as the voltage level. We implemented this pixel circuit layout in an area of $25\times25$ $\mu$m$^2$.

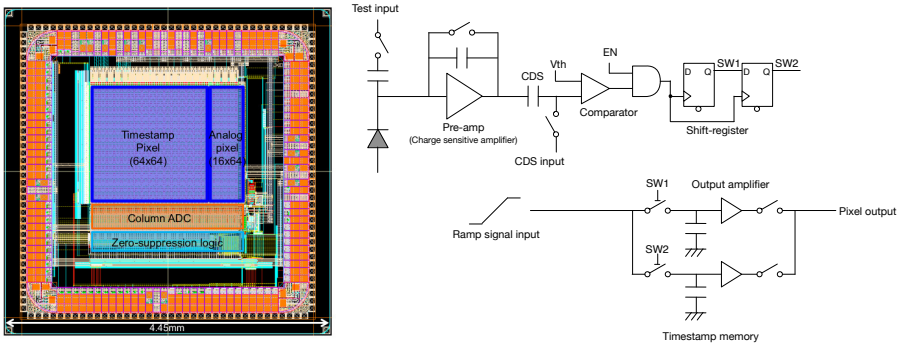


**Figure 6:** The chip overview (left panel) and Time-stamp pixel schematic (right panel) of SOFIST Ver.2.

The Ver.2 sensor is under fabrication. The Ver.2 sensor chip will be delivered at December 2016. We adopted a double-SOI wafer for the fabrication of Ver.2 sensor chip. The additional silicon layer also compensates the crosstalk between the analog and digital part in the pixel circuit [5].

## 4. Summary and Future prospect

We have been developing a monolithic pixel sensor SOFIST based on SOI technology for the ILC vertex detector. SOFIST stores both the position and timing information of charged particles. We are currently designing and evaluating two prototype sensor chips. SOFIST Ver.1 chip has a pixel circuit with analog signal readout and Ver.2 chip has a pixel with the in-pixel time-stamp function. We are planning the sensor evaluation for studying the sensor position resolution with high energy beam of the charged particle at Fermilab Test Beam Facility in December 2016.

After the evaluation of the Ver.1 and Ver.2 sensors, we will start the study of Ver.3 prototype sensor. The third pixel circuit has the function to store both the charge signals and timing information within a pixel area of $20\times20$ $\mu$m$^2$. We are planning the pixel circuit implementation with

3D stacking technology [6]. The Ver.3 chip will have additional circuit layer on SOI sensor chip (Figure 7). We can implement further circuits in one pixel by stacking circuit layers. The additional layers are connected electrically by advanced micro-bump technology, which can be placed with the fine pitch of 5 $\mu$m. This sensor chip will be submitted in 2017.

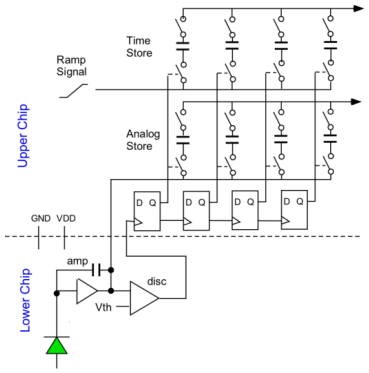


**Figure 7:** The pixel schematic of SOFIST Ver.3 with SOI 3D stacking sensor. The pixel circuit will have four analog signal memories and four time-stamps.

## 5. Acknowledgement

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