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Double-sided strip sensors for the Limadou-CSES project

Irina Rashevskaya*, **William Burger, Cristian Manea,**
INFN-TIFPA, Via Sommarive 14, 38123 Trento, Italia
E-mail: irina.rashevskaya@tifpa.infn.it

Maurizio Boscardin, Pierluigi Bellutti, Francesco Ficorella, Sabina Ronchin, Nicola Zorzi,
FBK, Via Sommarive 13, 38123 Trento, Italia

Luciano Bosisio, Giulio Orzan,
INFN-Trieste, Padriciano 99, 34149 Trieste, Italia

Gabriele Giacomini,
Brookhaven National Laboratory, 11973 Upton, NY, USA

Filippo Ambroglini, Giovanni Ambrosi.
INFN-Perugia, Via Alessandro Pascoli 06123 Perugia, Italia

The production of 71 AC-coupled double-sided silicon microstrip sensors, designed to equip the two layers of the High Energy Particle Detector (HEPD) detector in the Limadou-CSES (China Seismo-Electromagnetic Satellite) project, has been recently completed at FBK. The sensors, fabricated on 150 mm silicon wafers, have an overall size of 10.96 cm $\times$ 7.76 cm = 85.05 cm^2. Sensor testing and quality control has been performed at INFN Trieste and TIFPA. After presenting an overview of the test procedures and results, the contribution will focus on the analysis of some characteristic defects, which were severely limiting the production yield. As a result of this study, a modification of the fabrication process has been proposed, leading to an increased yield.

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*Speaker.

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1. Introduction

An important component of the scientific apparatus of CSES (China Seismo-Electromagnetic Satellite) is the High-Energy Particle Detector (HEPD), designed to detect electrons, protons and light nuclei. The main goal is to measure variations of the electron and proton fluxes due to short-time perturbations of the radiation belts caused by solar, terrestrial and anthropic phenomena, including seismic events of medium and strong intensity. The energy range explored is 3 - 100 MeV for electrons and 30 - 200 MeV for protons. Two planes of double-sided silicon microstrip detectors, placed on top of the HEPD, measure the direction of the incident particles. Each plane consists of six silicon sensors, assembled into three ladders, for a total sensitive area of about 23 cm $\times$ 22 cm.

Section 2 describes the sensor and the test procedures adopted. Section 3 reports a summary of the results of the quality acceptance tests. In Section 4 some characteristic defects, which were severely limiting the production yield, are analyzed; this study suggested a modification of the fabrication process, leading to an increased yield.

2. Sensor description and test procedures

2.1 Sensor description

The sensors[1], fabricated on 150 mm diameter, 300 μm thick silicon wafers, have an overall size of 10.96 cm $\times$ 7.76 cm, for a total area of 85.05 cm^2. They have 384 readout strips on *p*-side and 576 on *n*-side, both at 182 μm pitch, arranged orthogonally to each other. The readout strips are interleaved with floating strips, and all of them are biased by punch-through from a Bias Ring (BR). A single Guard Ring (GR) is present on *p*-side, intended to be left floating during operation of the detector; its purpose is to allow an easy separation of the active area current from the edge-generated current at the test level. The readout strips have integrated capacitors for AC-coupling to the readout electronics; the floating strips are non-metallized, but provided with DC contact pads at the ends.

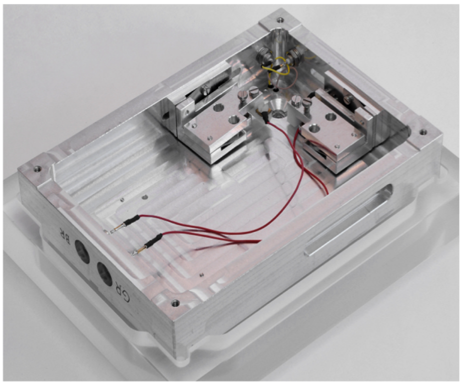
2.2 Measurement setup

A complete electrical test of each sensor is performed, making use of a semiautomatic probe station and of standard semiconductor characterization instruments (DC Source-Measure Units, LCR Meter).

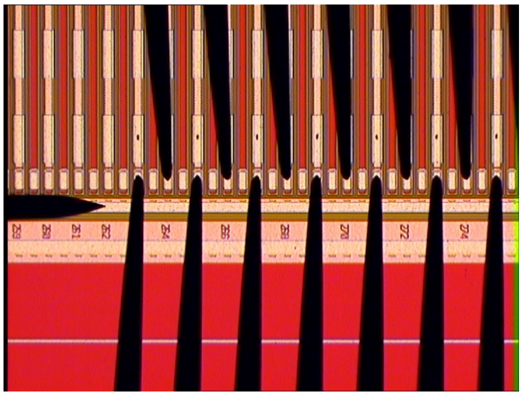
The double-sided sensor is first manually mounted on a custom-designed support. The Bias and Guard Rings on the back-side are contacted by miniature manipulators built into the jig (Fig.1a). Strips are contacted by a probe card with 50 needles arranged in line, at 182 μm pitch (Fig.1b). The probe card pitch is determined by the test of the AC capacitors, present only on the readout strips. When testing the 'implanted' or 'DC' strips, that have a pitch of 91 μm, the probe card contacts every second strip. On punch-through biased sensors this implies that during the DC scan the contacted strips are interleaved by strips that stay at a different voltage; as a consequence, the currents measured during the DC scan do not faithfully represent the strip currents expected during

[1]Produced by FBK, Trento, Italy.

normal operation of the detector, when all strips stay at the punch-through voltage with respect to the Bias Ring. Two rather extreme examples of these effects, occurring in association with fabrication defects, are discussed in Section 4. Measuring the 767 (384 readout + 383 floating) strips on the p-side requires 16 touchdowns of the probe card, while measuring the 1157 (576 readout + 575 floating) strips on the n-side requires 24 touchdowns of the probe card. Prober and instrument control, data acquisition and preliminary data analysis are performed with a suite of LabView programs[2] that allows the user to configure customized test sequences through a simple script language.



(a) A dedicated jig for testing double-sided sensors (view of the back-side with manipulators used to contact the bias and guard rings).



(b) View of the first 13 needles of the 50-needle probecard, contacting the p-side DC-pads. The single needle on the left makes contact to the bias ring.

Figure 1: Sensors testing setup.

2.3 Standard test sequence

The n-side of the sensor is tested first, since it is advisable to determine the n-side strip insulation voltage as early as possible within the test sequence. On each side, the 'AC strips' (integrated capacitors) are tested first, because of the possibility - although remote - that testing operations may degrade the quality of the underlying 'DC strips'[1].
The complete test sequence [2] on the n-side is the following one:

1) *AC Strip Scan.* Only the AC pads and the substrate (backside bias ring) are contacted. Every strip capacitor is measured sequentially, with a 20V bias applied across it. Capacitance, dissipation factor and leakage current are measured simultaneously, by making use of a custom-designed bias adapter. Capacitance is measured at 1 kHz frequency; the sensor is exposed to visible light in order to shunt the equilibrium depletion capacitance of the junction, which is in series with the oxide capacitance. This test, besides giving the capacitance value of every strip, allows detecting all defect types affecting the AC strips:
- Broken capacitors

[2]"M-Shell", developed and written by R. Wheadon, INFN Torino.

- Leaky capacitors
- Metal shorts between adjacent strips
- Metal opens (interruptions of the metal strip)

2) *$I-V$ Measurement.* The probe card is positioned on the DC pads, and the bias ring is contacted with a manipulator. An $I-V$ measurement is performed, with the bias voltage ranging from 1 to 100V. The currents of bias and guard rings on p-side (backside) are measured, together with the current of the n-side bias ring and of one n-side strips. The strip $I-V$ characteristics allow a quick and effective estimate of the insulation bias voltage, since parasitic currents due to instruments offset voltages dominate the measured strip current until good strip insulation is reached.

3) *Punch-Through Voltage Measurement.* Without moving the contacts, the punch-through voltage drop between bias ring and strip is measured for two different strips versus bias voltage [3].

4) *DC Strip Scan.* The contacts are already positioned for the start of the strip scan on DC pads. The bias voltage to be applied on the backside is chosen using as an input the insulation voltage determined in 2) for one strip. During the scan, the following parameters are measured:
- Leakage current of every strip.
- Insulation resistance of every strip (a 0.2V offset voltage is applied to the strip under test, and the resulting current change is measured).
- Bias ring current and backside current once for every probe card position (24 values).
- Strip insulation voltage of one strip for every probe card position. This is performed by starting from a low value of the bias voltage, and increasing it in 2V steps until the measured insulation resistance exceeds 100 MΩ.

The *AC Strip Scan* and *DC Strip Scan* are repeated on the p-side of the detector (except no strip insulation voltage is measured during DC scan).

3. Summary of qualification test results

The CSES-HERD Silicon detector consists of 12 silicon sensors arranged in two planes. Two different detectors have been assembled: a 'Qualification Module' (QM) to be used for testing purposes and a 'Flight Module' (FM), to be installed in the satellite.
- 71 sensors have been completely tested.
- 50 sensors have passed the acceptance test: 22 suitable for the QM and 28 for the FM.

The numbers and frequencies of the different defect types are reported in Table 1.

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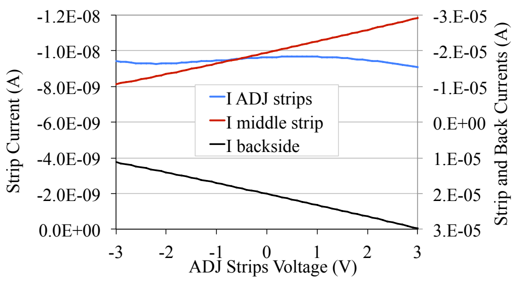
	Qualification Module		Flight Module	
	22 sensors		28 sensors	
Defect type	p-side	n-side	p-side	n-side
$I_{strip} > 20$ nA	14.6 (1.9%)	22.4 (2.0%)	1.6 (0.2%)	5.8 (0.50%)
Implant short	0.05 (0.01%)	0.00 (0.00%)	0.32 (0.04%)	0.36 (0.03%)
Broken capacitor	1.95 (0.25%)	12.4 (1.09%)	0.71 (0.09%)	8.14 (0.71%)
Metal short	0.32 (0.04%)	1.18 (0.10%)	0.75 (0.10%)	0.68 (0.06%)
Metal open	0.00 (0.00%)	0.05 (0.00%)	0.00 (0.00%)	0.00 (0.00%)
Total	**16.1 (2.1%)**	**35.3 (3.1%)**	**3.3 (0.4%)**	**14.5 (1.3%)**

Table 1: Statistics of the different defect types for the sensors passing the acceptance test for the two modules. The average number per sensor of each defect type and the percentage of affected strips are reported. The last row gives the total number (and the percentage) of defective strips per sensor.

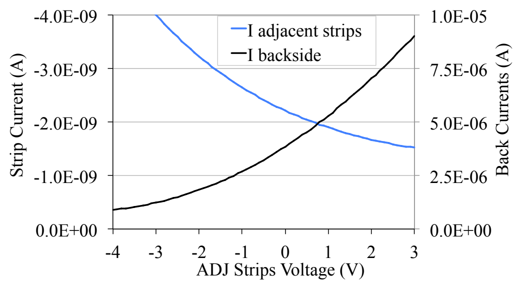
4. Failure analysis on some characteristic defects

4.1 P-side

A significant fraction of the sensors showed a high leakage current, increasing rapidly with bias voltage and reaching several tens of microamperes at 100 V bias. The DC scan of the strips showed that this current was in most cases due to a single *p*-side strip. The high current has been attributed to a low-voltage Zener-type breakdown between the p^+ strip and an accidental n^+ doped spot overlapping the edge of the strip. The potential difference between this *n*-type spot and the *p*-type strip – and hence the breakdown – is strongly influenced by the voltage of neighbouring strips. The accidental *n*-type region was thought to be created during the *n*-type diffusion process that was used for the ohmic contact on backside. Figure 2 shows that the current of the central strip and the total current of the sensor markedly increase when the adjacent strip voltage is made more positive:



(a) Current of middle strip (set at V = 0), adjacent strips and backside versus voltage of adjacent strips. All other strips floating. Vbias = 80 V.



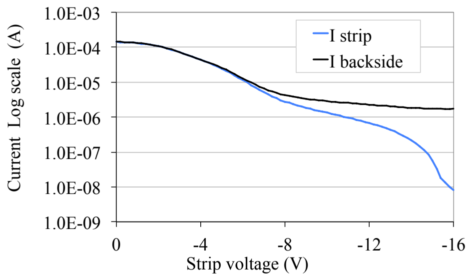
(b) Current of adjacent strips and backside versus voltage of adjacent strips, with middle strip floating (=> sitting at the punch-through voltage, about +3 V)

Figure 2: Dependence of the currents on the voltage applied to the strips adjacent to a high current *p*-side strip.

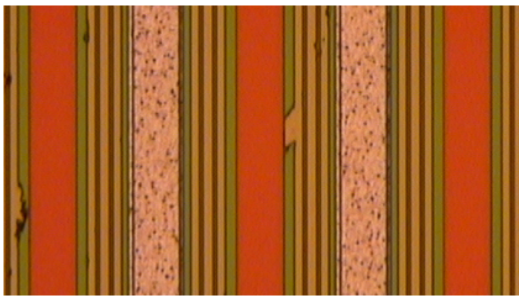
this has the consequence of increasing the voltage difference between the n^+ doped spot and the central p^+ strip. Following this interpretation, a change in the fabrication process for n^+ doping from diffusion to implantation has been proposed, which would make it impossible to accidentally dope the opposite face of the wafer. This change successfully prevented the occurrence of the very high current strips and lead to significant increase of the yield.

4.2 N-side

On some sensors, a high current was found to originate from a single *n*-side strip during the DC scan on *n*-side, but was not reflected in the I-V measurement made by contacting only the Bias Rings, with all strips biased by punch-through. Also in this case the high current has been attributed to a low-voltage Zener-type breakdown, here occurring between the n^+ strip and a *p*-stop which, due to a lithography defect, was overlapping the edge of the n^+ strip. This defect has been confirmed by optical inspection (Fig. 3b). At 100 V bias the *p*-stops sit at a voltage more negative than about –16 V w.r.t. the n-side Bias Ring. When the *n*-type strip is directly contacted it is forced to 0 V and the highly doped junction breaks down; electrons are collected by the *n*-strip and holes are injected by punch-through from the *p*-stop to the *p*-side strips. It must be noted that during normal operation of the sensor, when all n^+ strips are left floating so that they all sit at the same voltage determined by the punch-through mechanism, the high current disappears.



(a) Current of a defective *n*-type strip and backside (*p*-side) versus voltage applied to the defective strip, all other strips floating (=> sitting at the punch-through voltage, about -16 V)



(b) Microscope image showing a *p*-stop implant which extends up to the *n*-type strip at the center of the picture.

Figure 3: Dependence of the currents on the voltage applied to a defective *n*-side strip.

5. Conclusions

The quality and yield of these large-area double-sided sensors initially suffered from the very recent transition of the FBK fabrication facility from 100 mm to 150 mm wafer processing, mainly due to random defects originated from the handling of double-sided wafers. After a tuning phase and thanks to the feedback provided by test and failure analysis, good quality and yield have been obtained. The sensors selected for the Flight Module have a low defect density, well within specifications.

References

[1] I. Rachevskaia et. al, *Test and quality control of double-sided silicon microstrip sensors for the ALICE experiment*, Nucl.Instrum.Meth **A530** (2004) 59-64

[2] I. Rashevskaya et. al, *Qualification of a large number of double-sided silicon microstrip sensors for the ALICE Inner Tracking System*, Nucl.Instrum.Meth **A572** (2007) 122-124

[3] G. Giacomini, L. Bosisio, I. Rashevskaya, *Insulation Issues in Punch-Through Biased Silicon Microstrip Sensors*, Trans.Nucl.Sci. **63** (2016) 422-426