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Muon Trigger development toward High Luminosity LHC

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The high luminosity LHC designed for the peak luminosity of 7×10^{34} cm^{2}s^{-1} and integrated luminosity of 3000 fb^{-1} is scheduled from 2026. The trigger and readout system of the ATLAS detector is also upgraded to cope with the increased latency and the increased first level trigger rate. The sophisticated tracking-based muon trigger algorithm with the Thin Gap Chamber (TGC) and the Monitored Drift Tube detector (MDT) is introduced in the end-cap first level muon trigger to improve the momentum resolution in the hardware level. Sending all hit information from the on-detector electronics to the off-detector electronics in the counting room allows us to make sophisticated tracking trigger algorithm. The developments of the TGC front end board and the MDT mezzanine cards are keys of the tracking-based trigger. In this paper, the developments of the end-cap muon trigger electronics, in particular the developments of the font-end electronics, are reported.

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1. Introduction

The high luminosity LHC (HL-LHC)[1] is scheduled from 2026 to explore new physics by the direct searches for new particles and precise measurements of Higgs couplings and the other SM processes. The ATLAS detector[2] is also upgraded for the HL-LHC[3] and the technical design reports for this upgrade is published in 2017.

The detector for HL-LHC should be designed for the peak luminosity of 7×10^{34} cm^{2}s^{-1} and integrated luminosity of 3000 fb^{-1}. In HL-LHC, we expect that the rates for low energy QCD background evens as well as interesting events are increased, the average number of collisions per bunch crossing is increased to the level of 200, and the detector and electronics are exposed to more intense radiation. Therefore, the detector upgrade for HL-LHC is focused on the development of the advanced trigger and the data acquisition system and the replacement of the inner and the forward detectors. In this paper, the developments of the muon trigger upgrade in the end-cap region are reported.

2. Trigger and readout scheme

A new trigger and readout scheme which allows longer latency and higher trigger rate is essential to take full advantage of HL-LHC. In order to cope with the increased latency from 2.5 μs to 10 μs and the increased first level trigger rate from 100 kHz to 1 MHz, most of the electronics for the muon system have to be replaced by new ones. At the same time, the advanced trigger algorithm is developed to expand the acceptance of the interesting events with keeping the background rate low enough.

3. End-cap muon trigger upgrade

Current muon trigger measures the momentum of muons by using the coincidence of the hits from the muon detectors which are located at the most outer part of the barrel and the end-cap of the ATLAS detector[5]. The sophisticated tracking-based muon trigger algorithm is introduced from HL-LHC to improve the momentum resolution in the hardware level.

The end-cap muon trigger makes trigger decision using the deflection angle (β) between track segments provided by the inner and outer stations as shown in Figure 1. The New Small Wheel (NSW)[4] which is introduced in 2021 provides the track segments with 1 mrad resolution. The track trigger using the Thin Gap Chamber (TGC)[5] provides the track segments with 3 mrad resolution. The tracking trigger with Monitored Drift Tube (MDT)[5], which is newly introduced from HL-LHC provides the track segments with 1 m rad resolution.

4. Performance of the new muon trigger

The trigger rate study for the single muon trigger with 20 GeV threshold is emulated using the LHC Run1 data. Figure 2 shows the η distribution of the muons which are passed through the muon trigger condition of 20 GeV momentum threshold. If no muon trigger upgrade is introduces, muons distribute as the white histogram. On the other hand, offline selected muons with momentum truly

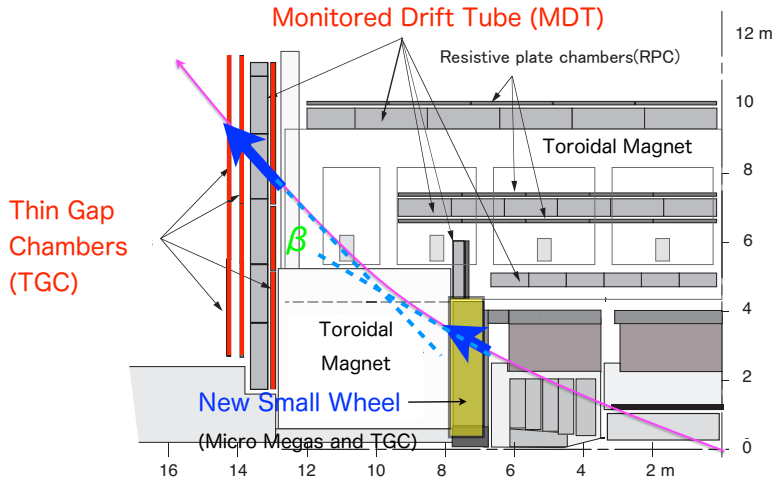

Figure 1: Algorithm of the end-cap muon track trigger.

greater than 20 GeV distribute as the green histogram. By applying the TGC track trigger, muons distribute as the red histogram. The trigger rate reduction by TGC tracking trigger is estimated to be about 30 % in the end-cap region. By applying MDT track trigger as well as TGC track trigger, muon distributes as the blue histogram. The trigger rate reduction by MDT tracking trigger is estimated to be about 50 % in $|\eta| < 2.4$. At this time, the efficiency of muons reconstructed as momentum greater than 20 GeV by offline is better than 95 %.

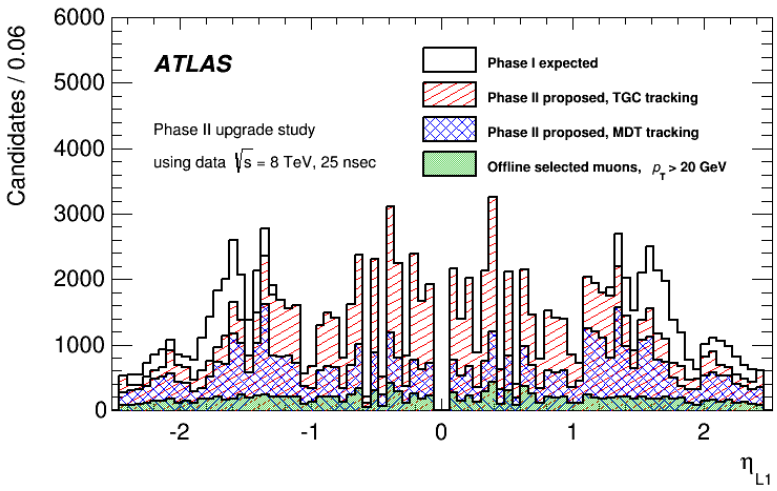

Figure 2: The performance of the muon trigger upgrade.

5. End-cap muon track trigger electronics

The end-cap muon tracking trigger with the TGC and the MDT is realized using the several electronics as shown in Figure 3. The hit signals from the TGC are digitized by Amp-Shaper-

Discriminator (ASD) ASIC. Digitized signals are fed into the TGC front-end board. The TGC front end board identifies which proton bunch crossing produces the TGC hit and transmits all TGC hits information to the off-detector electronics. The signals from MDT are fed into the MDT mezzanine card. The MDT mezzanine card digitizes the signals and provides the drift time information with the Time-to-Digital Converter (TDC). The chamber service module merges signals from mezzanine cards and transmits the MDT hit information to the off-detector electronics. The trigger algorithm is performed by the FPGAs or processors on the off-detector electronics in the counting room. Sending all hit information from the on-detector electronics to the off-detector electronics in the counting room allows us to make sophisticated tracking trigger algorithm. Therefore, the development of the TGC front end board and the MDT mezzanine cards are one of the key of the tracking-based trigger.

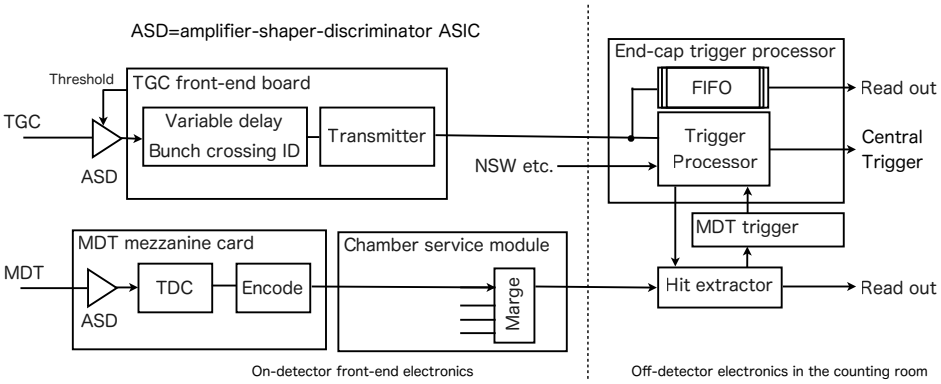

Figure 3: The diagram of the end-cap muon tracking trigger system with the TGC and the MDT.

5.1 Prototype of the TGC front-end board

Figure 4 shows the prototype of the TGC front-end board. A TGC front-end board can handle 256 TGC channels. This board has 8 Bunch crossing identification ASICs, a Kintex-7 FPGA, the Digital Analog Converters (DACs) and the Analog Digital Converters (ADCs) for the discriminator threshold, optical interfaces, and an Eithernet interface. A TGC front-end board needs to be achieved 16 Gbps data transfer using 2 optical fiber to send all TGC hit data to off-detector electronics. This board has all functionalities for HL-LHC upgrade. To fix the final design, bunch crossing id ASICs need to be replaced by new ones Operating devices (FPGA, DAC, ADC, regulator) in the intense radiation needs to be tested.

5.2 Demonstration of the TGC front-end board with the test beam

The TGC front-end board is demonstrated using muon test beams at the H8C beam line in CERN. Figure 5 shows the setup of the TGC chambers and the diagram of the electronics used for the beam test. The concept of the trigger and the readout scheme is same as a design for the HL-LHC. A prototype of the PS board handles only 256 channels of 4 layers of TGC around the beam spot.

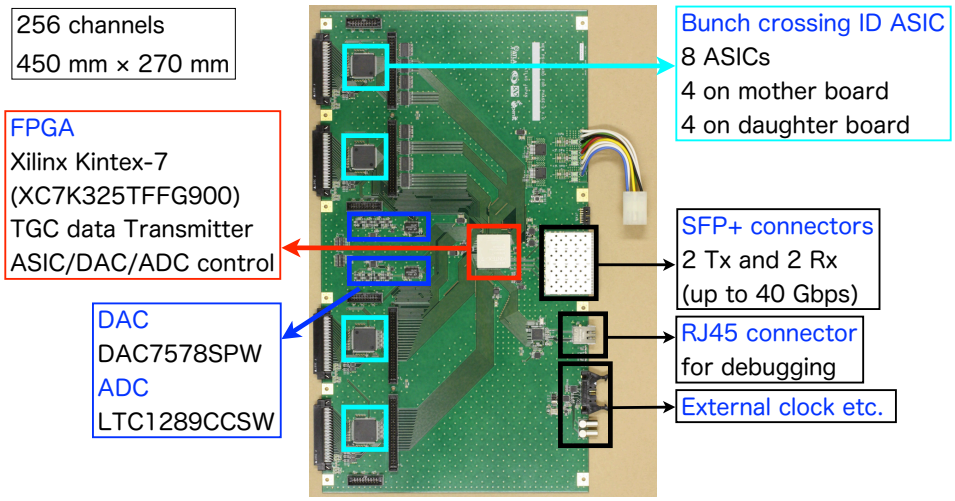

Figure 4: The picture of the prototype of the TGC front-end board.

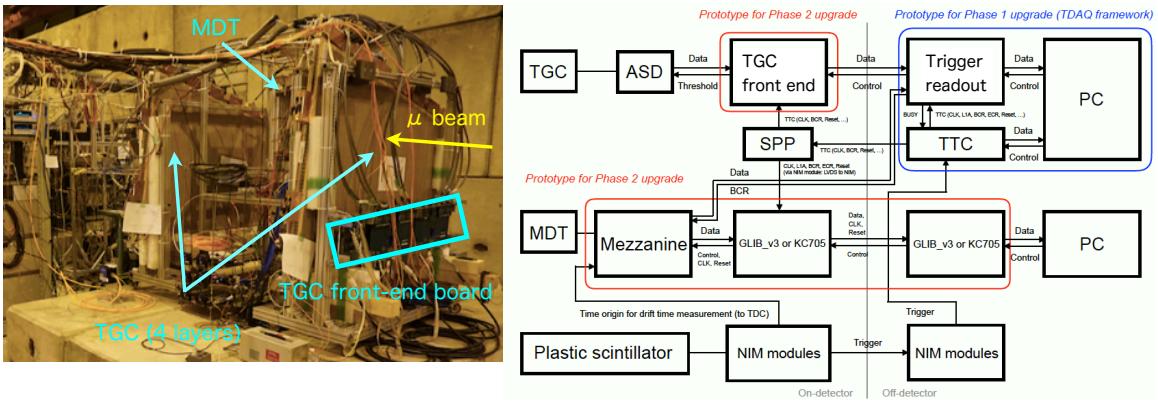

Figure 5: The setup of the beam test (Left) and the diagram of the electronics used for the beam test (Right).

Figure 6 shows linearity between the input voltage set to the DAC and the output voltage read out by a digital voltmeter. The ASD threshold can be set as one likes from the computer in the counting room. Figure 7 shows the map of the efficiency for the TGC hits with respect to the muon track. The efficiency is estimated from the events which have one hit for each layer other than the layer of interest. Most of the channels in the beam area has almost 100 % efficiency, while the efficiency is lower for some channels along the support structure of the wires inside the chamber shown by black lines in Figure 7. It indicates the validity of the data transferred by the prototype of the PS board. Thus, basic functionalities of the TGC front-end board have been demonstrated by the beam test.

5.3 Prototype of the MDT mezzanine card

Figure 8 shows the prototype of the MDT mezzanine card. This board can handle 24 MDT channels and has 3 ASD ASICs, a Kintex-7 FPGA for TDC, 3 input connectors from MDT, 1 LVDS

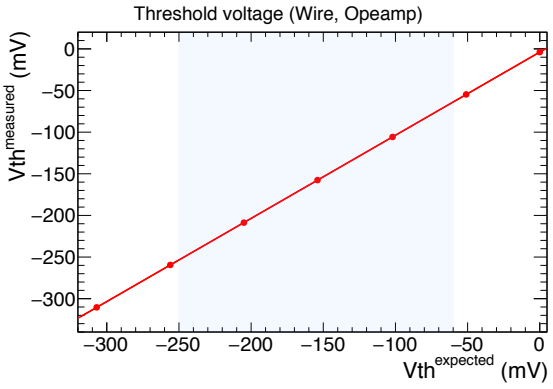

Figure 6: The linearity between the input voltage set to the DAC and the output voltage read out by a digital voltmeter.

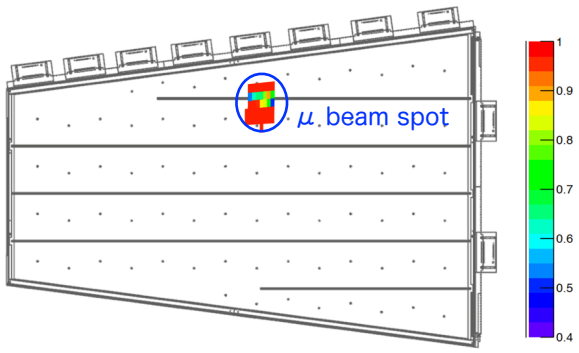

Figure 7: The map of the efficiency for the TGC hits with respect to the muon track.

copper connector for output. This board has all functionalities for HL-LHC upgrade. To fix the final design, the ASD ASICs need to be replaced by new one and the radiation-tolerant TDC device needs to be considered. We consider to develop the MDT mezzanine card with an ASIC-TDC as a baseline and to study the radiation hardness of the FPGA for the MDT mezzanine card with an FPGA-TDC as a backup option.

5.4 Performance of the FPGA-TDC on the MDT mezzanine card

Figure 10 shows the schematic of the TDC circuit on the FPGA. It is based on a multisampling scheme using quad phase clocks with the frequency of 320 MHz, which provide the bin size of 0.78 ns[8]. The quad phase clocks are synchronized with 40 MHz reference clock, which is assumed to use a clock from LHC. The time resolution is measured using test pulse to be 0.23 ns, which is equivalent to the quantization error ($= 0.78$ ns$/\sqrt{12}$). The linearity from 0.5 μs to 100 μs is confirmed. By raising reference clock up to 110 MHz, the TGC with the bin size up to 0.28 ns can be achieved. From these primitive measurements, we conclude that the digital part of the mezzanine card has been tested. Extracting drift-time information from the MDT analog hits is on going.

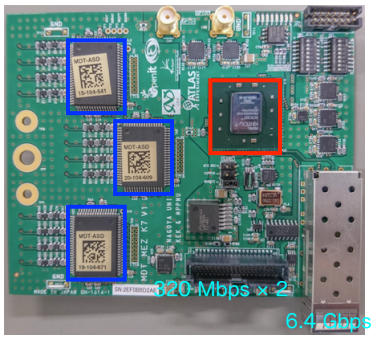

Figure 8: The picture of the prototype of the MDT mezzanine card.

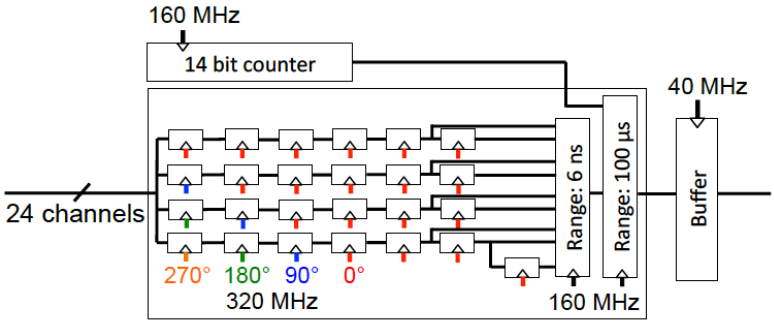

Figure 9: The schematic of the TDC cricuit on the FPGA.

5.5 Radiation test of the FPGA

Choosing radiation tolerant FPGA is crucial for the TGC and the MDT electronics upgrades. The SRAM type FPGA, for example Xilinx[6] Kintex FPGA, is expected to have high radiation tolerance against the total ionization dose (TID) up to 10 kGy while it is expected to have low radiation tolerance against the single event effect (SEE). On the other hand, The flash memory type FPGA, for example Microsemi[7] IGLOO2 FPGA, is expected to have relatively high radiation tolerance against the SSE. We produced a test board checking radiation tolerance of IGLOO2 FPGA. Using this module, the gamma-irradiation test has been performed and found that the firmware download got impossible within 100 Gy and the logics downloaded seems to survive with a higher does from 100 to 200 Gy. The TID at the muon detector location is estimated to be from 2 to 30 Gy after the integrated luminosity 3000 fb^{-1} is accumulated. Taking into account the safety factor about 20, the results of the radiation test indicates that the IGLOO2 FPGA can or cannot be used depending on the location of the front-end electronics. Further studies of the radiation tolerance of the FPGA , such as the radiation tolerance of IGLOO2 FPGA against SEE and the radiation tolerance of Kintex FPGA against TID and SEE is needed to choose the proper FPGA to be used for HL-LHC.

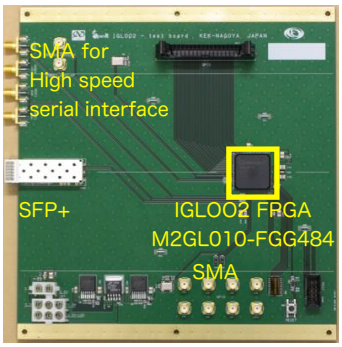

Figure 10: Test board checking the radiation tolerance of the Microsemi IGLOO2 FPGA.

6. Conclusion

The high luminosity LHC designed for the peak luminosity of 7×10^{34} cm^{2}s^{-1} and integrated luminosity of 3000 fb^{-1} is scheduled from 2026. The trigger and readout system of the ATLAS detector is also upgraded to cope with the increased latency and the increased firs level trigger rate. The sophisticated tracking-based muon trigger algorithm with TGC and MDT is introduced in the end-cap first level trigger to improve the momentum resolution in the hardware level. Sending all hit information from the on-detector electronics to the off-detector electronics in the counting room allows us to make sophisticated tracking trigger algorithm. The developments of the TGC front end board and the MDT mezzanine cards are keys of the tracking-based trigger. The prototype of the TGC front-end board is produced and demonstrated using the test pulse and the muon test beams at the H8C beam line in CERN. The prototype of the MDT mezzanine card is produced and measured the time resolution using the test pulse to be 0.23 ns. From these studies the functionalities of the TGC front-end board and the MDT mezzanine board are successfully demonstrated. The radiation tolerance of Microsemi IGLOO2 FPGA, which is the candidate to be used for HL-LHC upgrade, against TID is investigated. Further studies of the radiation tolerance of the FPGA, such as the radiation tolerance of IGLOO2 FPGA against SEE and the radiation tolerance of Kintex FPGA against TID and SEE, is needed to choose the proper FPGA tu be used for HL-LHC.

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