PROCEEDINGS OF SCIENCE

Development of a prototype front-end board of the Thin Gap Chamber for ATLAS at the High-Luminosity LHC

Tomomi Kawaguchi*
Nagoya University
E-mail: kawaguchi@hepl.phys.nagoya-u.ac.jp

Kotoko Shukutani
Nagoya University
E-mail: shukutani@hepl.phys.nagoya-u.ac.jp

The High-Luminosity LHC is planned to start the operation in 2026 with the increased luminosity of about 5×10^{34} cm^{-2}s^{-1} in order to provide more precise measurements of the standard model processes and to extend the reach for new particles. The trigger and readout electronics for the ATLAS experiment are planned to be replaced by new ones to cope with the higher event rate at the High-Luminosity LHC. The end-cap muon trigger plans to select the events using the deflection angle between the segments before and after the magnetic field. The Thin Gap Chamber (TGC) provides the segments after the magnetic field with 3 mrad angular resolution. In order to implement the new TGC trigger, the front-end boards of TGC need to send the hit data for all channels (∼320,000 channels) to the off-detector electronics. The prototype of the front-end board with the concept for the upgrade has been developed and demonstrated using muon test beam line at CERN. In this report, we introduce the prototype of the front-end board and the results of the beam test.

The 3rd International Symposium on "Quest for the Origin of Particles and the Universe"
5-7 January 2017
Nagoya University, Japan

*Speaker.

PoS(KMI2017)065

1. Introduction

High-Luminosity LHC (HL-LHC) is planned to start the operation in 2026 with the increased luminosity of about 5×10^{34} cm^{-2}s^{-1} in order to provide more precise measurements of the standard model processes and to extend the reach for new particles. In order to cope with the higher event rate for HL-LHC, the trigger and readout electronics for all subsystems need to be replaced by new ones [1]. At the same time, sophisticated trigger algorithm is planned to be introduced to suppress the events including muons with low transverse momentum. In this report, we focus on the improvement of the first level muon trigger algorithm in the end-cap regions.

2. Thin Gap Chamber Track Trigger

2.1 Thin Gap Chamber

TGC is a multi-wire proportional chamber [2]. Seven layers of TGC are located in the end-cap regions of ATLAS detector. Signals from the anode wires and the strips arranged orthogonal to the wires provide two-dimensional position measurements.

2.2 First Level Muon Trigger Algorithm

The current first level muon trigger algorithm is based on the coincidence of seven layers of TGC. On the other hand, that for the HL-LHC makes the decision using the difference of the angle β calculated by the deflection of a muon track at both of after and before magnetic field as shown in Figure 1. The New Small Wheel (NSW), which will be introduced in 2019-2020 provides the azimuth angle of the muon track with 1 mrad angle resolution before the toroidal magnetic field. TGC also provides that with 3 mrad angle resolution after the toroidal magnetic field using the simple tracking algorithm with hits from all TGC layers. The angle measurements provided by NSW and TGC improves the transverse momentum resolution of the muon. The performance studies show that the rate of the single muon trigger with p_{T} theshold of 15 GeV is reduced by 30% in the end-cap regions.

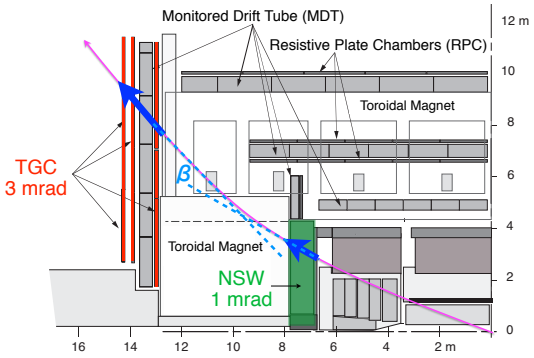

Figure 1: Algorithm of TGC track trigger

2.3 Concept of Trigger and Readout Electronics

Figure 2 shows the schematic of the TGC trigger and readout electronics for HL-LHC. Signals digitized by amplifier/shaper/discriminator (ASD) boards are fed into the TGC front-end board

(PS board). A PS board aligns the timing of the hits and identifies which proton bunch crossing produces the TGC hit information and transmits all hit data to the off-detector electronics. It allows us to make a sophisticated TGC track trigger. Moreover, the PS board controls and monitors the threshold voltage for the discriminator on the ASD board.

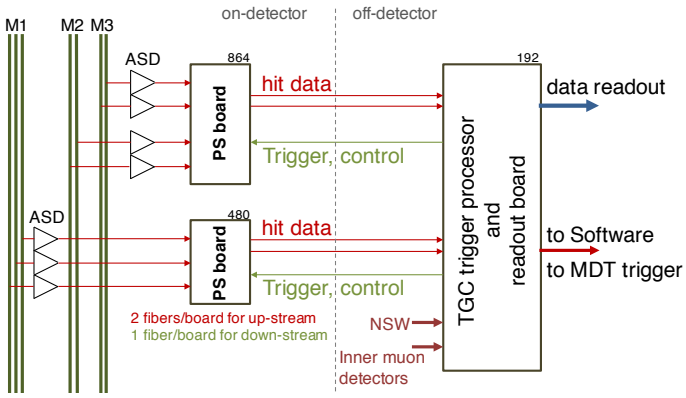

Figure 2: Concept of trigger and readout electronics

3. Prototype of TGC PS Board

A picture of prototype of the PS board for HL-LHC is shown in Figure 3. This board has 8 patch-panel ASICs for the timing alignment and bunch identification, DACs and ADCs for the control and the monitor of the ASD threshold, and an FPGA. The FPGA sends all TGC hit data to the off-detector electronics without selections. It configures the patch panel ASICs, DACs, and ADCs. This board communicates with the Trigger Timing and Controller (TTC) board using copper cables. The data is transferred to the trigger processor and readout board via two optical fibers. The prototype board has also an Ethernet interface for debugging.

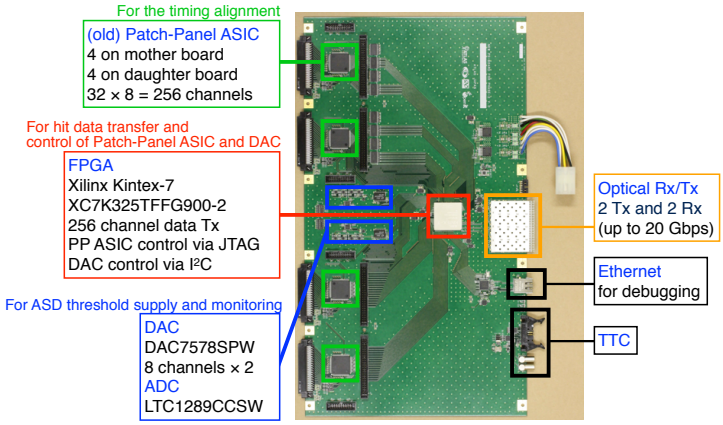

Figure 3: Prototype of PS board

4. Besic Performance Test

The data transfer of the PS board is demonstrated using test pulse. The firmware controlling the ASD threshold is developed and tested.

4.1 Demonstration of the Data Transfer

A PS board handles 256 channels of TGC. Taking into account 64 bits of headers and trailers and 8b/10b encoding, a PS board needs to send 400 bits to off-detector electronics in synchronization with 40 MHz LHC clock. The PS board is designed to transfer hit data by two optical fibers, each of which manages the transfer rate of 8 Gbps. We measured the bit error rate of the high-speed data transfer using Xilinx's IBERT [3] to be less than 8.91×10^{-15}.

4.2 Demonstration of the ASD Threshold Control

The circuit diagram for the ASD threshold control is shown in Figure 4. The set value and channel ID of DAC are transferred from the FPGA register on the TGC trigger processor and readout board to the PS board via an optical fiber. Thereafter, the FPGA on the PS board controls 2 DACs via I^2C buses, and then the ASD threshold is provided with an operational amplifier. In this way, negative and positive voltages are provided for wires and strips, respectively. Additionally the setting values on DAC can be readout by FPGA via the I^2C bus. Perfect linearity between the set and the measured value is obtained by the measurement of the ASD threshold with digital voltmeter.

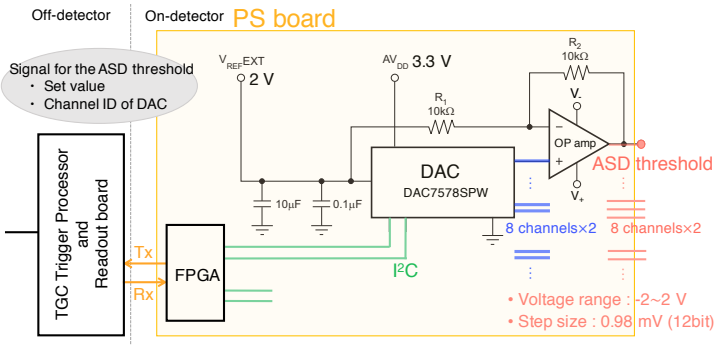

Figure 4: Schematic of the ASD threshold control

5. Demonstration with Muon Beams

A full TGC readout chain with the prototype of PS board has been demonstrated using muon beams at the H8 beam line in CERN. The main items of the demonstration are the ASD threshold control and the data transfer from the PS board to the off-detector electronics.
The setup of beam test is shown in Figure 5. Hit signals from 256 channels are transmitted with two optical fibers from the PS board to the TGC trigger processor and readout board (data transfer rate: 8 Gbps $\times$ 2 = 16 Gbps). The signals are then transmitted to PC. The control signals for the ASD threshold is transmitted from PC to the TGC trigger processor and readout board. They are thereafter transferred to the PS board by an optical fiber.

In order to verify the data transferred by the prototype of PS board, we checked the efficiency for each channel. It has been estimated from the events which have one hit for each layer other than the layer of interest. The result of efficiency study is shown in Figure 6. Most of the channels in the beam area has almost 100% efficiency. However, the efficiency is lower for some channels

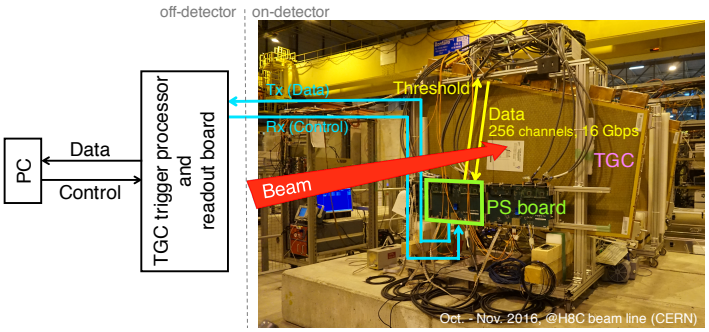

Figure 5: Setup of the beam test

along the support structure of the wires inside the chamber shown by black lines in Figure 6. It indicates the validity of the data transferred by the prototype of the PS board. Furthermore, the ASD threshold control based on FPGA is verified. Therefore, basic functionalities of the PS board have been demonstrated.

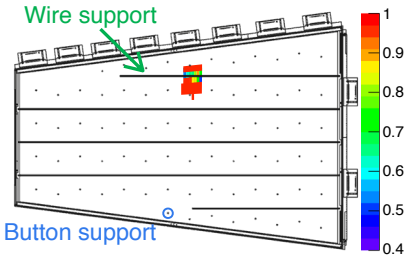

Figure 6: Efficiency and the TGC support structure

6. Conclusion

A prototype of the PS board for HL-LHC has been developed. The PS board for HL-LHC is required to manage the hit data transfer to the off-detector electronics with a rate of 16 Gbps and the ASD threshold control. The data transfer of the PS board is demonstrated using test pulse. We measured the bit error rate of the high-speed data transfer to be less than 8.91×10^{-15}. The firmware controlling the ASD threshold is developed and tested. Perfect linearity between the set and the measured value is obtained by the measurement of the ASD threshold. In addition, a full TGC readout chain with the prototype of PS board has been demonstrated using muon beams. We checked that the data transferred by the prototype of the PS board is correct and the ASD threshold control based on FPGA is also verified. Therefore, the prototype of PS board has been successfully demonstrated.

References

[1] The ATLAS Collaboration, "ATLAS Phase-II Upgrade Scoping Document", CERN-LHCC-2015-020

[2] ATLAS Muon Collaboration, "ATLAS Muon Spectrometer Technical Design Report", CERN/LHCC 97-22

[3] Xilinx Inc, https://www.xilinx.com/