

FPGA Implementation of AES Algorithm Resistant Power Analysis attacks

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In order to be more effectively resist differential power analysis attacks, the improved fixed value masking algorithm is proposed for resource-constrained smart card based on fixed value masking and random masking. Firstly, a number of random numbers are selected and prestored in on-chip ROM for generating the corresponding byte-substitution table. It does not increase much power and hardware resources because the byte-substitution table is pregenerated. Finally, experiments in terms of the second-order differential power analysis attacks have been carried outon the improved fixed masking. The experimental results show that the proposed AES algorithm can be effectively resistant to the side-channel attacks with lower computing expenses and higher security.

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1.Introduction

At present, the password security of all kinds of smart cards have achieved the people's concerns and attention.SCA(Side Channel Attacks) was proposed in one paper[1], which completely broke the traditional way of cipher algorithm algebra brute force Attacks. The SCA depends on the leakage power consumption during the process of encryption, time and physical information such as electromagnetic radiation, which can decipher the key at a very low cost. The safety smart card needs to enhance the protection method in the design and technical research of implementation against the side channel attacks [2].

2. Improvement of the Fixed Value by Masking AES algorithm and the Optimized Implementation

2.1 Mathematical Proof of the Masking AES Algorithm Resistant to the ide-Channel Attacks

Plaintext P_t masks by using the random number *m*, key represents the encryption key to mask the keys with random number m_k . The byte substitution operation in AES algorithm needs a corresponding amendment, satisfies the new byte substitution:

$$SubBytes'(x+m) = SubBytes(x) + m'$$
(2.1)

After the mask, key and plaintext are output from the changing S-box: $S'[(P_t + m) + (key + m_k)] = S'[P_t + key + m + m_k] = S[p_t + key] + m_s$ (2.2)

where ms=m+ mk

Without the masking byte substitution operation, if there is a guessed value k of the key, there is output byte substitution $S[P_t] + k$. With the output of the No.b value as the classification function, n power curves V_{ii} can be divided into two groups as follows:

$$V_0(S[P_t + k]) = \{V_{ii} \mid D_b(S[P_t + k]) = 0\}$$
(2.3)

$$V_1(S[P_t + k]) = \{V_{ii} \mid D_b(S[P_t + k]) = 1\}$$
(2.4)

Due to the randomicity of plain text input, each digit probability of 1s and 0s is 50%. You can think of the two groups of size n / 2. For each group, on average, after subtracting the received j^* time differential curve for the power consumption of the DPA:

$$T[j^*] = \frac{2}{n} \{ \sum_{V_{ij}} V_{ij} \in V_0(S[P_t \oplus key]) - \sum_{V_{ij}} V_{ij} \in V_1(S[P_t \oplus key]) \}$$
(2.5)

Set the probability that the No.d bit value of a number x is 0 as $\beta_d(x)$. As the exclusive-OR with 0 does not change the original value, the probability that the No.d bit of $S[p_t] + k$ equals to the No.d of $S[p_t] + k + m_s$ is $\beta_d(m_s)$. Rewrite the equation above:

$$T[j^{*}] = \frac{2}{n} \{\beta_{d}(m_{s}) \frac{\sum V_{ij}}{V_{ij} \in V_{0}(S[P_{t} \oplus k] \oplus m_{s})} + (1 - \beta_{d}(m_{s})) \frac{\sum V_{ij}}{V_{ij} \in V_{1}(S[P_{t} \oplus k] \oplus m_{s})} - (1 - \beta_{d}(m_{s})) \frac{\sum V_{ij}}{V_{ij} \in V_{1}(S[P_{t} \oplus k] \oplus m_{s})} = \frac{2(2\beta_{d}(m_{s}) - 1)}{n} \{V_{ij} \in V_{0}(S[P_{t} \oplus k] \oplus m_{s}) - V_{ij} \in V_{1}(S[P_{t} \oplus k] \oplus m_{s})\} \}$$

$$(2.6)$$

From Equation (2.6), if $\beta_d(m_s)$ is 0.5, i.e. The probability of an arbitrary number of 0 is 0.5, the peak amplitude $T^*[j]$ is 0, which prove that a random number masking method can resist side channel attacks by means of mathematical formalization.

2.2 Design Idea about Optimization

There are many added methods of random masking AES algorithm, including fixed value look-up table method, the improved fixed value look-up table method, multiplicative masking method, simplified multiplication masking method, embedded multiplication mask, etc. Partial methods are still not completely resistance to side channel attack, such as multiplication masking method with security risk of an attack by zero value, at meanwhile, the majority masking added methods have higher resource usage and are not suitable for resource-constrained smart card equipment safety. This paper proposes the improved fixed value look-up table method based on the fixed value look-up table method [3].

For the disadvantage of the look-up table method, that there are 256 values of the random number "m" with eight bits, and there are 256 new byte substitution form accordingly. If the encryption by using a random number each time is not fixed, the corresponding byte substitution must be quickly provided. If the method of fixed generation is used, you must store these tables to improve the computing speed. There are 256 kinds of tables, each table contains 256 values, the area consumption in the smart card development design is not acceptable. If the look-up table is generated randomly, it will consume speed and power and decryption time is basically spent in byte substitution table generation, which is clearly unacceptable by smart card producers and consumers.

With these defects, we put forward an improved fixed value masking algorithm, in which we chose a few fixed random numbers at the outset to produce a few bytes substitution tables stored in advance, then selected number randomly from the several fixed possible values during encryption. As the byte substitution tables are generated in advance, the area consumption is not too much and the speed of fixed value masking look-up table is fast. The diagram of the implementation in this way is shown as follows:



Figure 1: Framework of the Improved Fixed Value Masking Algorithm

The implementation method of the fixed value masking algorithm is described in detail as follows. Extract a few fixed values mask from a random number according to the strength of encryption key chip. The following is the implementation method of masking algorithm [4-6] in which three random Numbers are extracted as the fixed value:

Algorithm 1 Improved fived value AFS algorithm .	
Input: .	
Plaintext P.	
Output:.,	
Γ.	
1. Call GenerateRandoNumber() to generate three randomly number r0 ,r1 and r2, where r0 ,r1 ,r2 \in	[0,q-1];
2. Let lm[0]=mr0, lm[1]=mr1, lm[2]=mr2;	
3. Call GenerateRandoNumber() to generate randomly number s, s \in [0, 1, 2, 3];	
4. T'←Pt,	
5. $T' \leftarrow ApplyMask(T',r);$	
6. $T' \leftarrow T' \bigoplus K^{0}$.	
7. for i=1 to Nr do	
8. $T' \leftarrow ByteSub_FM(T',r[s]);$	
9. $T^{*} \leftarrow shiftRow(T^{*});$	
10. $T^* \leftarrow MixColumn(T^*);$	
II. $T' \leftarrow T' \oplus K';$	
12. end for,	
13. T'= ByteSub FM(T'.r[1]);,	
14. T'=shiftRow(T');.,	
15. $T'=T' \oplus KNr_i$.	
16. T=ApplyMask(T',r);,	
17.return T.	

2.2 Generation of S-box

To effectively and correctly generate the S-boxes, you need to write the program to automatically generate a new S box. The flow diagram of S-boxes generation is as follows in Figure 2:



Figure 2: Framework of S-box

2.3 Core Code of AES Algorithm

Keep the original basic framework of AES algorithm code, the ciphertext XOR mask, select the corresponding mask S-box for the S-box, do exclusive-OR of the state and mask at last input so as to recover the standard cipher text.

input:

always @(posedge clk) sa33 <= #1 ld_r ? text_in_r[007:000]^ w3[07:00]^ 8'h11: sa33_next; always @(posedge clk) sa00 <= #1 ld_r ? text_in_r[127:120]^w0[31:24]^ 8'h11: sa00_next; the output: always @(posedge clk) text_out[127:120] <= #1 (dcnt==0)?text_out[127:120]^ 8'h11:sa00_sr ^ w0[31:24]; always @(posedge clk) text_out[007:000] <= #1 (dcnt==0)?text_out[007:000]^ 8'h11:sa33 sr ^ w3[07:00];

With the random algorithm, the amended S box added corresponding mask can achieve the standard implementation of fixed value algorithm.

2.4 Experiment Results

The improved fixed value masking AES algorithm can be simulated with modelsim6.1f function correctly, the result of simulation waveform is shown as follows in Figure 3.

				.a4eooob	1003dC47	303/4/3	7060360	<u>, I Döözla</u>	arizaerci	DIDU/34,	.564eD4e	1131836	7603FFC3,	63C4eU0
						×								
000102030	4050607080	90a0b0c0d	0e0f											
													(
001122334	4556677885	9aabbccdd	eelf											

Figure 3: Waveform of the Improved Fixed Value Masking AES Algorithm

The simulation results are shown in Figure 4.



Figure 4: Output of the Improved Fixed Value Masking AES Algorithm

3.The implementation of the improved fixed value of masking AES algorithm on FPGA

3.1 The FPGA Implementation

After the hardware language of the improved fixed value masking AES algorithm, it is downloaded to the FPGA. The final running results are shown in Figure 5.

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key: D4D1C6F8 7C839D87 CAF2B8BC 11F915BC result: 371F3F06 2C50A66C F97563B8 ECC39A34 Encrypting in round 7 state: 371F3F06 2C50A66C F97563B8 ECC39A34 key: 6D88A37A 110B3EFD DBF98641 CA0093FD result: 4B5053A0 858CD0E B2F10874 6B9D151D Encrypting in round 8 state: 4B5053A0 858CD0E B2F10874 6B9D151D key: 4E54F70E 5F5FC9F3 84A64FB2 4EA6DC4F result: FB924DE1 1554223C 744C89BC 9487A1D4 Encrypting in round 9 state: FB924DE1 1554223C 744C89BC 9487A1D4 key: EAD27321 B58DBAD2 312BF560 7F8D292F result: FA51E30F 483F2995 9AB002F6 AD253C3 key: AC7766F3 19FADC21 28D12941 575C006E result: 3925841D 2DC09FB DC118597 196A0B32

Figure 5 : Improved Fixed Value Masking AES Algorithm on FPGA

The downloaded operation figure can verify that the results of the corresponding design are correct.

3.2 Experiments of Resistance to Power Analysis Attack

The experiments of resistance to the second-order differential power attack have been carryied out with the improved fixed value mask AES algorithm and a fixed value masking algorithm respectively. As the basic idea of experiment, first of all, the IP core of the fixed value mask and the improved one are implemented respectively to simulate the function operation of IP core, then extract the inversion of 1-0 and 0-1. The inversion directly corresponds to the change of the power curve during encryption key chip operation. By means of software programming and automatic statistical analysis according to the principle of the bypass attack, we conclude the results in Figure 6 and Figure 7.

The experimental results of a fixed value mask second-order differential power attack are shown in Figure 6.



Figure 6 : Attack's Results of A Fixed Value Mask Order DPA

The experimental results of the improved fixed value mask second-order differential power consumption attack are shown in Figure 7.



Figure 7: The 2-order DPA Results of the Improved Fixed Value Masking

From Figure 6 and Figure 7, we know the result that a fixed value mask is unable of resisting the second-order differential power consumption attack, which is consistent with the validated results in other literature, while the improved fixed value mask can resist the second-order DPA.

4. Conclusion

The mask method resistant to the side-channel attack is profoundly studied in this paper. With the widespread use of smart card, its security has attracted the people's wide attention and research. A smart card is resource-constrained device, and its size and operation ability are limited. This paper proposes an improved method of fixed value mask based on the fixed value mask, describes the specific hardware implementation in detail, and verifies the corresponding experimental results. Based on the experiment results, we can conclude that the improved fixed value mask algorithm highlights better performance than the fixed value mask algorithm in resistance to side-channel attack with less increase of resource consumption.

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