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# KM3NeT Front-end electronics upgrade: CLBv3 and PBv3

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**on behalf of the KM3NeT collaboration**

High efficiency, high reliability and low power consumption are the main challenges for the design of the front-end electronics of the KM3NeT neutrino telescope. The so-called Phase II of the KM3NeT project, to be started after the completion of the ongoing Phase I, is currently under design. It presents an opportunity to enhance the performance of the front-end electronics. The present article describes the main modifications under study for the KM3Net Phase II front-end electronics boards, the Central Logic Board and the Power Board. These modifications aim for a higher efficiency and reliability, and a lower power consumption and price.

*35th International Cosmic Ray Conference – ICRC2017*
*10-20 July, 2017*
*Bexco, Busan, Korea*

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## 1.- Introduction

The KM3NeT neutrino telescope is currently in construction in the Mediterranean Sea [1]. The main objective is the discovery and observation of the high energy neutrino sources of the Universe. The Cherenkov photons induced by muons created by the interaction of neutrinos in the surrounding of the detector and propagating at a speed higher than light in the medium, are collected by a 3-D matrix of light detectors, the so-called photomultipliers (PMTs). From the arrival times of the Cherenkov photons and the position of the PMTs, the muon track, which is highly correlated with the neutrino originating the muon, is reconstructed.

The PMTs are housed in a glass vessel called Digital Optical Module (DOM). A total of 31 PMTs, distributed along the sphere of the DOM, collect the Cherenkov photons and convert them into electrical pulses. The electrical pulses are digitized and transferred to the Time-To-Digital Converters (TDCs) embedded in the Field Programmable Gate Array (FPGA) of the Central Logic Board (CLB), which is the main electronics board of the DOM. The TDCs measure the arrival time of the pulses as well as the pulse length (Time over Threshold or ToT) with a precision of one nanosecond; the information is then sent to the on-shore station via the optical link. The expected rate counting of photons is in the range of 5 to 10 kHz per PMT, which implies a data bandwidth of a few Mbits per second in each DOM. In order to synchronize the different DOMs the CLB implements the White Rabbit protocol [2], which allows sub-nanosecond synchronization.

The main electronics component of the Digital Optical Module of KM3NeT is, therefore, the Central Logic Board (CLB). Currently, the CLB and its associated Power Board (PB) are being redesigned for the Phase II of the KM3NeT infrastructure. The main goals of this redesign are: fixing of some minor flaws of the previous versions, improving of the reliability and decreasing of the power consumption and price.

## 2.- Hardware

### 2.1- PBv3

PBv3 is the latest version of the PB. It has been designed in 4 layers and it implements a few improvements with respect to the previous version, the PBv2. Several of the rails have been optimized. The DC/DC converter of 3.3 V had an efficiency of 65% in the previous version of PB. In order to increase the efficiency, this DC/DC converter has been changed to a model of the same manufacturer but with a better efficiency in the working point, which provides an efficiency of 90%. Similarly, the DC/DC of 2.5 V had also an efficiency of the 60%. Using a new model of DC/DC, the LTM8021, the efficiency increased up to 80%. The last rail optimized is the one supplying the piezo, which works at 5 V: from an original efficiency of 60 %, again after changing the DC/DC model, from the Murata OKL -T/1 to the MAX 17542G, an improvement of 30% has been obtained, reaching an efficiency of 90%. In table 1 the changes from PBv2 to PBv3 are summarised. Moreover, the PBv3 implements the possibility to add a fuse at the input of the board. Finally, the reliability has been improved going from a FIT value of 947 in the PBv2 version down to a FIT value of 783 in the PBv3 version, which means an improvement of 17.3%.



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| V (V) | I (A) | Efficiency (PBv2) | Type of DC/DC (PBv2) | Replacement in PBv3 | Efficiency (PBv3) |
|---|---|---|---|---|---|
| **2.5** | **0.125** | **60** | **OKL-T/1** | **LTM8021** | **80** |
| 3.3 | 0.33 | 90 | OKL-T/1 | OKL-T/1 | 90 |
| **3.3** | **0.335** | **65** | **OKL-T/3** | **OKL-T/1** | **90** |
| 1 | 0.8 | 80 | OKL-T/3 | OKL-T/3 | 80 |
| 1.8 | 0.46 | 80 | OKL-T/1 | OKL-T/3 | 80 |
| **5** | **0.1** | **60** | **OKL-T/1** | **MAX17542G** | **90** |

**Table 1.** Summary of the efficiencies of the different rails in PBv2 and PBv3.

### 2.2- CLBv3

The CLBv3 version of the CLB implements 12 layers (6 signal layers, 2 power planes and 4 ground planes). All layers have been symmetrically routed around the 2 power layers. The ground planes have been routed isolating the signal layers in order to achieve a better signal integrity. As in the CLBv2, the TDC differential pairs have been routed keeping the differences in propagation time below 100 ps while the clock signals have been routed with differences lower than 20 ps.

One of the main modifications of the CLBv3 is the use of a new FPGA, the ARTIX 200, which has a lower power consumption and a lower price with respect to the KINTEX-7 FPGA used in the CLBv2. Compared to KINTEX-7, an ARTIX 200 is a slightly slower FPGA which makes timing closure of the firmware design a challenge.

The design includes the installation of two different clock systems, both of which will be operative and available for tests, enabling a change from one to the other clock system via firmware configuration.

When implementing White Rabbit, two external oscillators (one reference clock generator and one Dual Mixer Time Difference (DMTD) clock generator) are necessary [3].

The previous CLBv2 version used oscillators which operated in the 20 and 25 MHz range that were synthesized to 125 MHz and 124.992 MHz using a PLL. For the CLBv3 phase noise is minimized by avoiding frequency synthesis and selecting very low phase noise oscillators (CVPD-922, [4]) that directly supply the frequencies needed.

The quality of these oscillators should be fully exploited. Therefore, a new ADR4525 reference is used which is an ultra low noise reference with only 1.25 uVp-p noise between 0.1-10 Hz and provides better stability than the LM336 used in the previous version of the CLB. For the same reason special attention has been given to the routing of the White Rabbit oscillators.

The compass and tilt sensors, that were previously present in a daughter board, the so-called AHRS, have been integrated directly on the CLBv3 PCB, together with a pressure sensor, a



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novelty with respect to the previous version of the CLB. The CLBv2 and the block diagram of CLBv3 are shown in Figure 1.

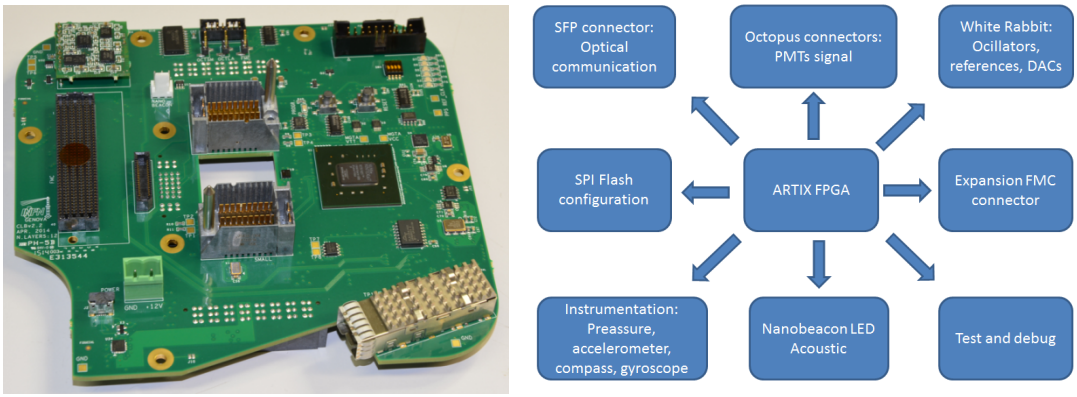


**Figure 1** a) CLBv2 b) Block diagram of CLBV3

As for CLBv2, the CLBv3 will undergo a FIDES analysis for evaluating the risk of failure in 15 years. Several signal integrity simulations were also performed on different signals on the board, showing a good discrimination level.

### 3. Conclusions

In this article, the main upgrades applied to the CLBv3 and the PBv3, which are under study for use in the Phase II of the KM3NeT infrastructure, have been presented. The aims have been to rely on a better design with higher reliability, lower power consumption and lower price. Moreover, the minor flaws of the previous version have been corrected.

### Acknowledgment

The authors acknowledge the financial support of the Spanish Ministerio de Ciencia e Innovación (MICINN), grants FPA2009-13983-C02-01, FPA2012-37528-C02-01, ACI2009-1020, Consolider MultiDark CSD2009-00064, YC-2012-10604, European Community's Sixth Framework Programme under contract nº 011937 and the Seventh Framework Programme under grant agreement nº 212525 and of the Generalitat Valenciana, Prometeo/2009/

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