

# Mini-EUSO photodetector module data processing system

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**A. Belov**

*Lomonosov Moscow State University, Skobeltsyn Institute of Nuclear Physics (SINP MSU),  
Moscow, Russia*

*Lomonosov Moscow State University, Faculty of Physics, Moscow, Russia*

*E-mail: aabcad@gmail.com*

**P. Klimov**

*Lomonosov Moscow State University, Skobeltsyn Institute of Nuclear Physics (SINP MSU),  
Moscow, Russia*

*E-mail: pavel.klimov@gmail.com*

**F. Capel\***

*KTH Royal Institute of Technology, Stockholm, Sweden*

*E-mail: capel@kth.se*

**M. Bertaina, F. Fausti, M. Mignone**

*Department of Physics, University of Torino and INFN Torino, Italy*

**for the JEM-EUSO Collaboration**

Mini-EUSO is a UV telescope which is developed by the JEM-EUSO collaboration to be placed on board the International Space Station (ISS) to carry out measurements of UV atmosphere airglow and transient luminous events (TLEs) in a wide field of view ( $>40^\circ$ ) and high temporal resolution ( $2.5 \mu\text{s}$ ). Mini-EUSO is developed to be a space qualified pathfinder of future JEM-EUSO missions. Optical system of the detector consists of two Fresnel lenses of 25 cm diameter. The focal surface is composed of 36 produced by Hamamatsu multi anode photomultiplier tubes (MAPMT), each with 64 pixels. The output signal of all 2304 pixels is digitized and then passed to the data processing system that was specially developed for the experiment and is being discussed in this work. Data processing system is based on produced by Xilinx ZYNQ chip that contains both programmable part (FPGA) and processor. Such combination in a single chip gives a big advantage for processing a data gathered from focal surface including fast multi-level trigger algorithms, data buffering, MAPMTs high voltage control algorithms, interfaces with front-end electronics and with the separate central processor unit for data storage. The multi-level trigger was developed for the mini-EUSO instrument to perform measurements in various time scales (temporal resolutions  $2.5 \mu\text{s}$ ,  $320 \mu\text{s}$ ,  $40 \text{ms}$ ). This trigger was successfully implemented and tested.

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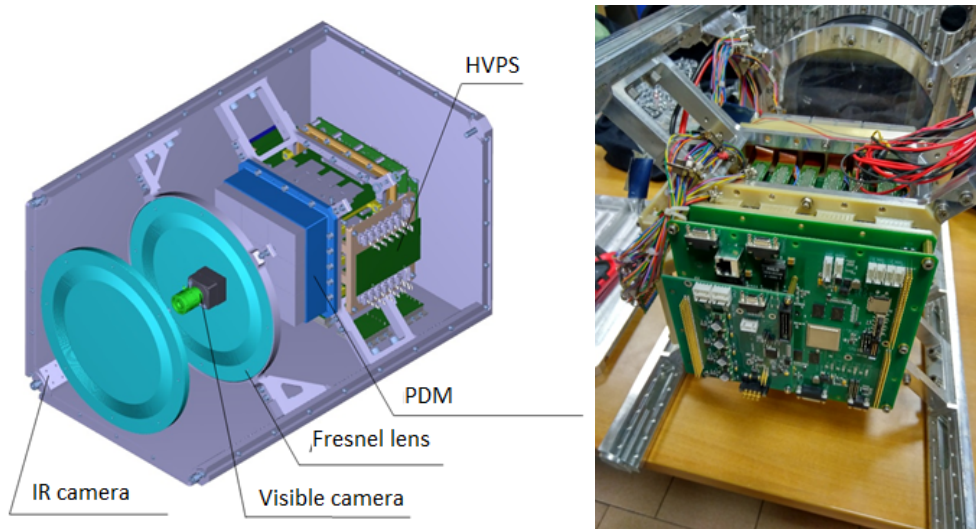
\*Speaker.

## Introduction

The Mini-EUSO telescope is designed for the measurement and mapping of the UV night-time emissions from the Earth and is being developed by the JEM-EUSO Collaboration as a pathfinder for the detection of extreme energy cosmic rays (EECRs, those with energies  $>50 \text{ EeV}^1$ ) from space such as KLYPVE-EUSO [1, 2] on the Russian Segment of the International Space Station (ISS) and JEM-EUSO [3]. The Mini-EUSO mission is a joint project between Italy and Russia, was selected by the Italian Space Agency (ASI) and is supported by the National Institute of Nuclear Physics (INFN); then, under the name “UV atmosphere”, it was approved by the Russian Space Agency Roscosmos and included in the long-term program of space experiments on the ISS. The launch of Mini-EUSO is programmed from late 2017 to early 2018.

The detector is a wide field of view telescope composed of two Fresnel lens optical system of 25 cm diameter, the photo detector module (PDM) placed in a focal plane, consisting of 36 Hamamatsu Multi Anode Photo Multiplier Tubes (MAPMTs), ancillary detectors (visible and near infra-red cameras). In the left panel of fig. 1 the 3D model of Mini-EUSO is shown. More detailed description of the instrument can be found in [4, 5].

The front-end electronics is based on the ASIC (SPACIROC3 [6]) and boards developed for the JEM-EUSO, central processor unit (CPU) is a standard PCIe/104 form factor single board computer. PDM data processing (PDM DP) system is designed specifically for the Mini-EUSO and sufficiently differs from the previous EUSO projects (EUSO-TA, EUSO-Balloon and EUSO-SPB). What follows is a description of a new PDM DP hardware and software.

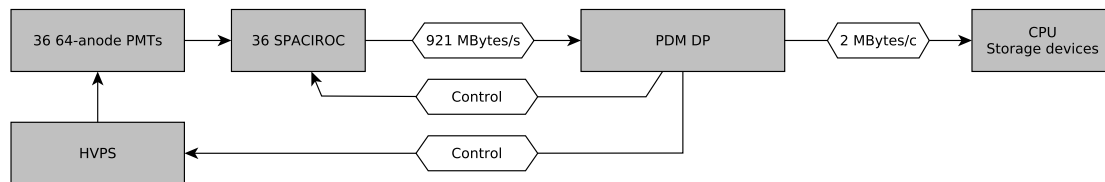


**Figure 1:** Left panel: The Mini-EUSO instrument 3D model. Right panel: the PDM-DP boards in the Mini-EUSO engineering model during tests.

<sup>1</sup>  $1 \text{ EeV} = 10^{18} \text{ eV}$ .

## 1. PDM-DP functionality

UV photons focused onto the Mini-EUSO focal surface are detected by the 36 MAPMTs and each PMT is read out by a 64 channel SPACIROC3. This data is digitised for each of GTU (gate time unit,  $2.5 \mu\text{s}$ ). The PDM DP performs the data gathering from photo detectors through SPACIROCs chips, the data preprocessing for detecting events (trigger algorithms) and the recording corresponding data fragments to the storage device. Input data flow is 961.2 MBytes per second ( $64 \text{ pixels} \times 36 \text{ PMTs} \times 400 \text{ k frames per second}$ ). Output data flow is limited by CPU performance and storage capacity. It's small in respect to input data flow and generally must be less than 2 MBytes per second. Also the PDM DP performs SPACIROC chips slow control configuration (i.e. setting the gains and analog voltage thresholds) and controls high voltage power supply (HVPS). The simplified data passing diagram in PDM block with data flow specification represented in fig. 2.



**Figure 2:** Simplified data passing diagram.

The incoming to PDM data flow speed is relatively high – almost 1 gigabyte per second. The data processing of so high flow is possible only using FPGA (Field programmable gate array), because it allows to implement parallel calculations. The trigger algorithms are commonly implemented inside FPGA. In case of successful triggering of the event an information about it and related input data should be sent to CPU for the further storage. For ease of interfacing with the CPU the Ethernet protocol TCP/IP has been selected. To implement fast data analyses and data transmission the so called System on chip (SoC) which is a composition of FPGA and processing system in one chip was chosen. It allows to realize all algorithms in one chip, simplify the development of the equipment and decrease the total power consumption of the system. PDM DP module has been designed using Xilinx ZYNQ 7000 chip. The chip consists of two main parts – programmable logic (PL) and processing system (PS).

Since trigger algorithms take some time to generate an event, it is necessary to store the input data stream (buffering) during this time. When an event occurs after a certain time the recording in the buffer is stopped. Then the information from the buffer is read out and sent to the storage device. This allows to provide measurements of UV intensity before and after a trigger. When the sending is complete, the system waits for new events to appear. The speed of writing data to the buffer must be greater than the data rate. In our case, the write speed should be at least 921.6 MB/s. The PDM DP uses external dynamic memory DDR3, which provides a continuous recording speed of up to 1600 MB/s. The memory capacity is 1 GB, which allows to save the input stream for a long time up to 1 s.

## 2. PDM DP structure

The PDM DP consists of three board - ZYNQ board, Cross board and Power board (it can be seen in the right panel of the fig. 1). On the ZYNQ board SoC ZYNQ chip, external memory DDR3, physical level Ethernet chip are placed. The Cross board is required for FPGA pins expansion. It contains 3 synchronised Xilinx Artix7 FPGAs which perform data gathering from the ASICs, pixel mapping and data multiplexing. Power board contains DC/DC converters and microcontroller for the voltage sequencing. Simplified diagram is presented in fig. 3. On this diagram is depicted which functional elements are connected to PS, and which are connected to PL of the ZYNQ.

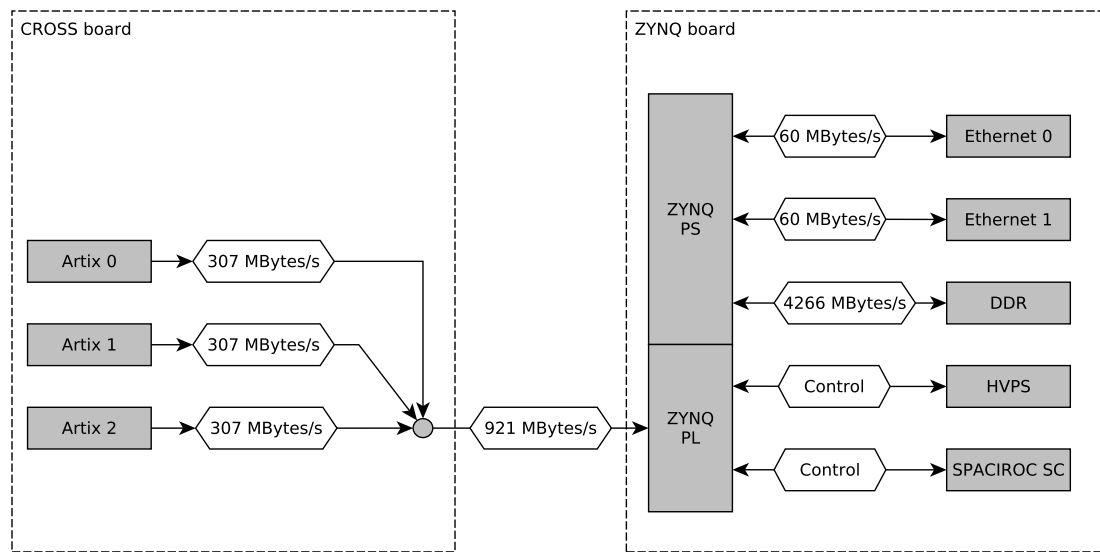


Figure 3: PDM DP diagram.

## 3. The multi-level trigger

The Mini-EUSO trigger algorithm is implemented in Hardware Description Language (HDL) inside the PL of the ZYNQ board and consists of two levels, L1 and L2, that work with different time resolution. Each level is dedicated to a specific category of events that will be observed by Mini-EUSO. The motivation behind the trigger algorithm is to measure different events in various timescales, but also to provide continuous imaging of night UV on around the Earth with 40 ms temporal resolution. In order to achieve this efficiently, 3 different types of data are stored with different time resolution. The L1 trigger gives data with a time resolution of  $2.5 \mu\text{s}$  and looks for signal excess on a timescale of  $20 \mu\text{s}$ , as this corresponds to the timescale of EECR like events. Each pixel is considered as independent, motivated by the fact that its field of view at ground is  $\sim 6 \text{ km}$ , so light takes at least  $\sim 20 \mu\text{s}$  to cross one pixel. Pixel signal is integrated over 8 consecutive GTUs and compared with the background level, determined over 128 GTUs, to look for an excess. If the signal is  $8\sigma$  above background, the event is triggered, the information from

the whole focal surface is read out and a packet of 128 GTUs is stored, centred on the trigger. This mode is needed to measure in the same time scale as planned for K-EUSO and JEM-EUSO experiment to understand well the UV signal structure, amplitude and possible sources of fake EECR triggers.

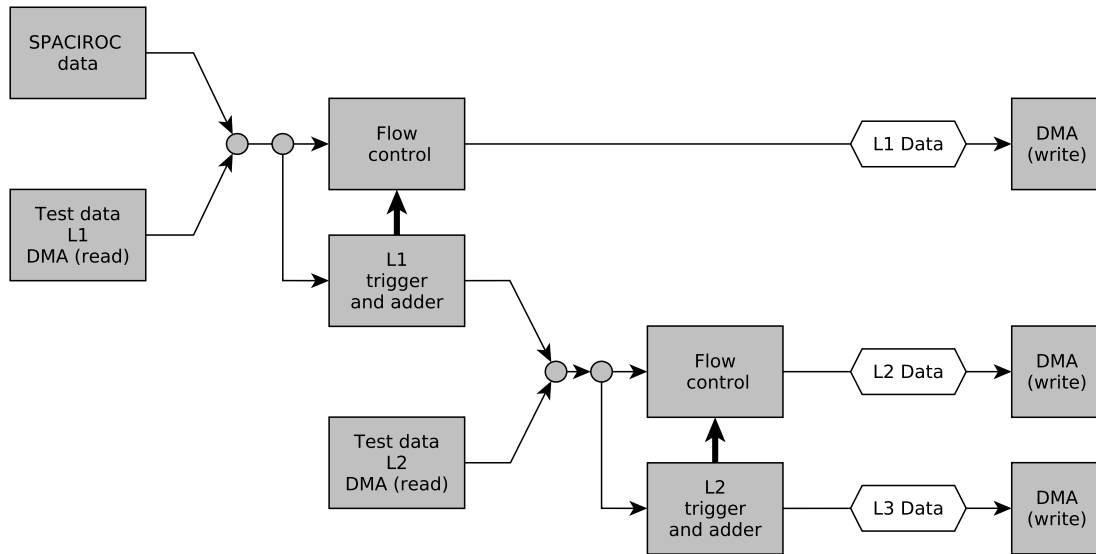
In addition to this, the data integrated over 128 GTUs ( $320 \mu\text{s}$ ) in order to set the background level, is then passed to the L2 trigger. The L2 trigger receives the integration of 128 GTUs ( $\text{GTU}_{L2}$ ) as input from the L1. It operates with a similar logic, but with a time resolution of  $320 \mu\text{s}$ , well-suited to capturing fast atmospheric events, such as TLEs and lightning, which have timescales of 1 – 100 ms. Background is set by integrating 128  $\text{GTU}_{L2}$ , which is also stored as the level 3 (L3) data, or 1  $\text{GTU}_{L3}$ . An L2 trigger occurs when the signal in 8  $\text{GTU}_{L2}$  is 4 times greater than the background level, and the event is stored. After the accumulation of 128  $\text{GTU}_{L3}$ , or every 5.24 s, all stored events from L1, L2 and L3 data are transferred to the CPU for formatting and storage on the disk. If no L1 or L2 events are triggered, instead the last 128 GTUs or 128  $\text{GTU}_{L2}$  present on the overwritten buffer are read out. In this way, a continuous and controlled readout is achieved with a resolution of 40.96 ms whilst also capturing interesting events at faster timescales. This 40.96 ms “movie” will be used to search for meteors, space debris and strange quark matter using offline trigger algorithms, as well as for the mapping of the Earth in UV.

#### 4. Memory management

The data path structure in ZYNQ firmware for Mini-EUSO is shown in fig. 4. The firmware can work in two modes: normal and test mode. In the normal mode the main data source is SPACIROCs. In the test mode the source is Direct memory access (DMA) block which provides the test data from specified external memory region.

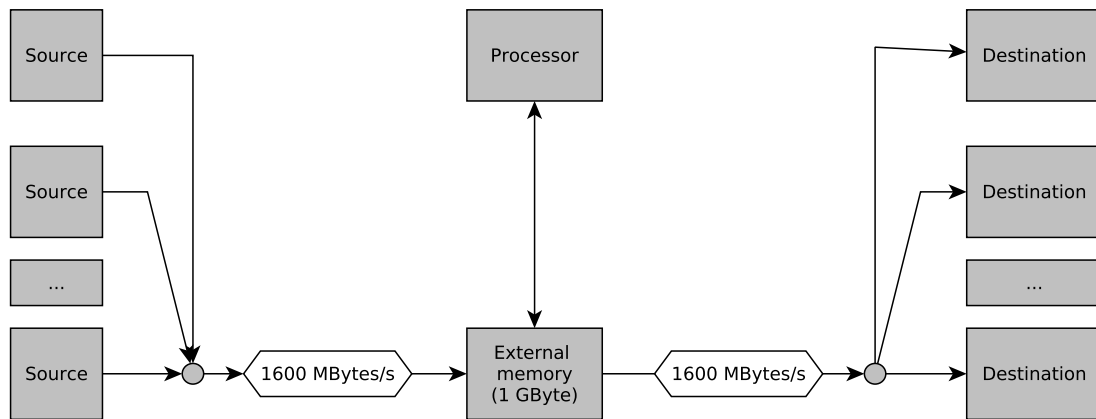
In the main mode the data from SPACIROCs passes in parallel to the L1 trigger block and to the Flow control block. The L1 trigger block generates trigger pulses (solid arrow on Fig. 4) and continuously produces the integrated data (thin arrow). Flow control block is needed to block the recording process. In case of L1 event is occurred the Flow control stops the L1 data flow after the specified time (not immediately) in order to include 128 GTUs of data after trigger. The management of the L2 data flow is similar as L1. Input data for L2 can be taken either from the L1 output port (integrated data) or from the L2 test data source. L2 trigger generates the trigger signal (solid arrow) and continuously produces the double integrated data (thin arrow). The last one is L3 data which is recorded continuously without triggering (“movie”).

The high rate of data and different types of memory requires a specific memory management for the detector. There are two memory types in PDM DP – block memory (BRAM - totally around 1 MB) and external memory DDR3 (1 GB). BRAM is placed inside ZYNQ and can be represented as more than 200 BRAM blocks of 4 kB each. BRAMs are used in the trigger algorithms and also as small data buffers. External DDR3 memory is connected to the ZYNQ PS, has significantly larger capacity, however has less throughput in respect to BRAM. Input data buffer is implemented on DDR3, because BRAM has insufficient size. An access from PL to external memory is organized using DMA. It allows to perform simultaneous read from several address ranges in memory and simultaneous write to memory from several data sources. The PS uses memory in parallel with



**Figure 4:** Data path structure in ZYNQ firmware for Mini-EUSO.

DMA read and write. The DMA read and write throughput is 1600 MB/s. The principle of DMA is depicted in Fig. 5.



**Figure 5:** The principle of DMA in ZYNQ.

Work with memory through DMA is widely used in Mini-EUSO (fig. 4). Before switching the system to the test mode corresponding memory regions must be filled with test data that will be applied to the input instead of SPACIROC data. The data taken from simulation models and from other experiments can be used as test data. There are two DMA blocks as test data sources presented in firmware – for L1 and L2 testing.

DMA approach is used also for the data recording. There are three DMA blocks for recording the data to memory (fig. 4). In the idle mode when firmware is waiting for new events the writing

DMA blocks are working continuously. It means that data is recorded into the circular buffers in memory. Flow control block in the idle mode is in “pass” state. When cyclic recording in the external memory is stopped, the processor program copies the corresponding data block and restarts the system waiting for the new event.

## 5. Conclusion

A digital data processing system (PDM DP) for Mini-EUSO was developed. The basis of PDM DP is a system on chip ZYNQ (Xilinx), which includes both FPGA and processor system. The PDM DP collects data from the photodetector devices, performs the two-level selection of events (trigger), their sending via Ethernet to the storage device, control of the high voltage power supply and the configuration of SPACIROC. In the period of 5.24 seconds, processing of 8 triggers of each level of event selection is possible. The multi-level trigger performs measurements in various time scales (temporal resolutions  $2.5\mu\text{s}$ ,  $320\mu\text{s}$ ,  $40\text{ms}$ ). The PDM DP of the focal surface of the EECR detector KLYPVE-EUSO on board the ISS will be based on the system presented here.

## Acknowledgments

We dedicate this proceeding to Yoshiya Kawasaki and Jacek Karczmarczyk, who passed away in 2016.

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