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New electronics for the surface detectors of the Pierre Auger Observatory

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The surface detector array of the Pierre Auger Observatory consists of 1660 water-Cherenkov detectors that sample at the ground the charged particles and photons of air showers initiated by energetic cosmic rays. Each detector records data locally with timing obtained from Global Positioning System (GPS) units and power from solar panels and batteries. In the framework of the upgrade of the Auger Observatory, AugerPrime, new electronics has been designed for the surface detectors. The electronics upgrade includes better timing with up-to-date GPS receivers, higher sampling frequency, increased dynamic range, increased processing capability, and better calibration and monitoring systems. It will also process the data of the AugerPrime scintillator detectors. In this paper, the design of the new electronics will be presented and its performance will be discussed in light of results from test measurements and from the engineering array data analysis.

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1. Introduction and design objectives

The surface detector (SD) of the Pierre Auger Observatory, located near Malargüe, Mendoza Province, Argentina, consists of an array of 1660 water-Cherenkov detectors (WCD) read out by three large XP1805 photomultipliers (PMT). The Collaboration is planning an upgrade of the detector that includes the addition of a scintillator-based surface detector (SSD) atop each WCD, together with an upgrade of the surface detector electronics (SDE) to both improve the performance of the existing detector and to provide an interface to allow the scintillator detectors co-located with the SD stations to make use of the data processing and communication infrastructure of the stations. The SDE records the PMT signals, makes local triggering decisions, sends timestamps to the central data acquisition system for the global triggers, and stores event data for retrieval when a global trigger condition is satisfied. These functions are implemented in a single board, called the upgraded unified board (UUB). Because of the small bandwidth (1200 bits/s) available to each tank, the station must operate semi-autonomously, performing calibrations and taking action in response to alarm conditions at the station level. The current SDE was designed 15 years ago using the technology available at that time. Evolution in processors, power consumption of electronics components, and timing systems make it possible today to design and implement a higher performance electronics system for the surface-detector array. The design of the current detector and its electronics is discussed in [1].

The design objectives of the new electronics globally aim to increase the data quality by faster sampling for ADC (analog-to-digital converter) traces, by better timing accuracy, and by increased dynamic range; to enhance the local trigger and processing capabilities by using more powerful local-station processor and FPGA (field-programmable gate array); and to improve calibration and monitoring capabilities of the SD stations. Backwards-compatibility with the current dataset will be maintained by retaining the current timespan of the PMT traces and providing for digital filtering and downsampling of the traces to emulate the current triggers in addition to any new triggers. The design objectives also aim for higher reliability and easy maintenance. A detailed description of the AugerPrime design can be found in [2].

An engineering array (EA) with 12 AugerPrime prototype detector stations was deployed on the Observatory site in October 2016 and has allowed us to verify the performance of the new electronics. In the following, the main features of the AugerPrime electronics are described. The performances based on the first EA data are discussed in [3].

2. Front-end and timing

The anode channel of the large XP1805 PMTs is split and amplified to have a gain ratio of 32. The signals are filtered and digitized by commercial 12 bit 120 MHz flash ADC (FADC). The pulse response of the XP1805, when expressed in terms of bandwidth, is ∼70 MHz. This is well matched to a 120 MHz FADC and associated 60 MHz Nyquist filter. We have chosen to use commercial 12 bit 120 MHz AD9628 FADCs, which achieve this performance with minimal power consumption, an important consideration due to the 10 W station-power budget.

A design goal of AugerPrime is to measure shower properties at energies above 6×10^{19} eV as close as 250 m from the shower core. For this purpose the WCD is equipped with an additional small photomultiplier tube (SPMT), a 1 inch Hamamatsu R8619 PMT, dedicated for the unsaturated measurement of large signals. The SPMT signal is also digitized with 12 bits at 120 MHz in a separate channel. The SPMT gain and the amplification are set such that the dynamic range is extended by a factor of at least 30 to about 20,000 VEM (vertical equivalent muon).

The anode channel of the SSD PMT is split; one is amplified to have a gain ratio of 32 and the other one is attenuated by a factor of 4. This yields a total gain ratio of 128. The signals are filtered and digitized similarly to the WCD PMT signals. The expected dynamic range for the SSD is 20,000 MIP (minimum-ionizing particle).

The calibration of the large PMT signals is performed by using background muons. The cross-calibration between the large PMTs and the small PMT is performed either by using small shower events or the existing LED flasher system that is adapted for brighter light pulses. A more detailed discussion on the dynamic range can be found in Ref. [4]. All the front-end functions as well as the LED (light-emitting diode) controller are directly implemented on the UUB to avoid connectors.

Synchronization of the detectors is provided by disciplining a local clock using the global positioning system (GPS). For the upgraded electronics we have selected the I-Lotus M12M timing GPS receiver manufactured by I-Lotus, LLC (Singapore). The M12M timing receiver is designed to be functionally compatible with the Motorola Oncore UT+ GPS receiver that is used with the current electronics. Choosing a compatible unit requires fewer and simpler modifications to the basic time-tagging system design. Specifically, the M12M provides the same 1 PPS (pulse per second) timing output with serial control and data. The specified intrinsic device accuracy after the applied granularity correction (the so-called negative sawtooth) is about 2 nanoseconds. This accuracy is very good relative to the UUB specification to achieve better than 5.0 ns RMS accuracy. The fundamental architecture of the time-tagging firmware module parallels the time-tagging design concept used in the current electronics and is implemented in the UUB board FPGA. The on-board software for initialization of the time-tagging modules, GPS hardware control, and timing data is similar to the current one, with minor modifications needed for the new UUB hardware.

3. Slow control and calibration

The UUB is equipped with a micro-controller (MSP430) for the control and monitoring of the PMT's high voltage, the supervision of the various supply voltages and reset functionality. For that purpose it controls 16 logic I/O lines, steers a DAC (digital-to-analog converter) with eight analog outputs and senses through multiplexers up to 64 analog signals with its internal ADC. The MSP430 also provides a USB (universal serial bus) interface and is tied via an I^2C-bus to an EEPROM (electrically-erasable programmable read-only memory) and a pressure sensor. More than 90 monitoring variables - including currents and voltages of the power supply and the PMTs - are managed by the slow-control software.

The VEM signal is the reference unit of the WCD high-gain calibrations, and was determined on a test tank with an external trigger hodoscope to give on average 95 photoelectrons at the cathode of the XP1805 PMTs, corresponding roughly to 150 integrated ADC counts above pedestal after signal digitization. The calibration of the low-gain channel compared to the high-gain channel is purely electronic and has an accuracy of better than about 2%.

The SSD calibration is based on the signal of a minimum-ionizing particle going through the detector. Since this is a thin detector, the MIP will not necessarily be well separated from the low-energy background but, being installed on top of the WCD, a cross-trigger can be used to remove all of the background. About 40% of the calibration triggers of the WCD produce a MIP in the SSD. Similarly to the WCD, the cross-calibration between high-gain and low-gain channels is defined by the electronics.

In addition to routine calibrations with physics events, each WCD is equipped with two LEDs. While these are not stable sources of calibrated light, they are very useful for monitoring and for linearity tests. These LEDs can also be used for the SSD.

4. Main electronics board

The various functions (front-end, calibration, time tagging, trigger, monitoring) are implemented on a single board, the UUB. An architecture with an FPGA containing an embedded ARM processor is used. The general architecture of the UUB is shown in Fig. 1.

The heart of the UUB is a Xilinx Zynq FPGA with two embedded ARM Cortex A9 333 MHz microprocessors. It is connected to a 4 Gbit LP-DDR2 memory and 2 Gbit flash memory. The FPGA implements all basic digital functions like the readout of the ADCs, the generation of triggers, the interface to the LED flasher, GPS receiver, clock generator and memories. High-level functions like the data handling and the communications with the radio transmitter are implemented under LINUX.

The speed of the upgraded CPU will be $>$10 times faster than that of the current one, with a similar increase in memory. This will allow much more sophisticated processing in the local station. The addition of accessible trigger IN/OUT and GPS 1 PPS signals will simplify time synchronization with other possible additional detectors. Furthermore, the high-speed USB will facilitate interfacing them. The current local-station software has been ported to LINUX. The data acquisition will be simplified by extending the use of FPGA firmware.

The trigger and time-tagging functionalities are implemented in the FPGA. The current local triggers (threshold trigger, time-over-threshold trigger (ToT), multiplicity of positive steps (MoPS) trigger, etc) will be adapted to the 120 MHz sampling rate. The increased local processing capabilities will allow new triggers to be implemented such as asymmetry-based triggers, and combined SSD and WCD triggers. The current muon memories and scalers will be retained. The trigger scheme includes the ability to down-sample and filter the data to the current 40 MHz rate which will allow the detectors to be operated with the new electronics emulating the current system. This will allow deployment of new electronics during the maintenance of the current system without disturbance to the data taking.

The UUB will be installed in the current enclosure with a new front panel. Two digital connectors are provided for possible additional detectors. These connectors provide 8 differential lines, each of which can be individually defined as input or output in the FPGA. An example of such allocation could be: trigger out, clock out, PPS out, busy in, data in, sync in, data out, sync out, etc. Moreover, this connector will provide unregulated +24 V, switched and limited, with a current monitor.

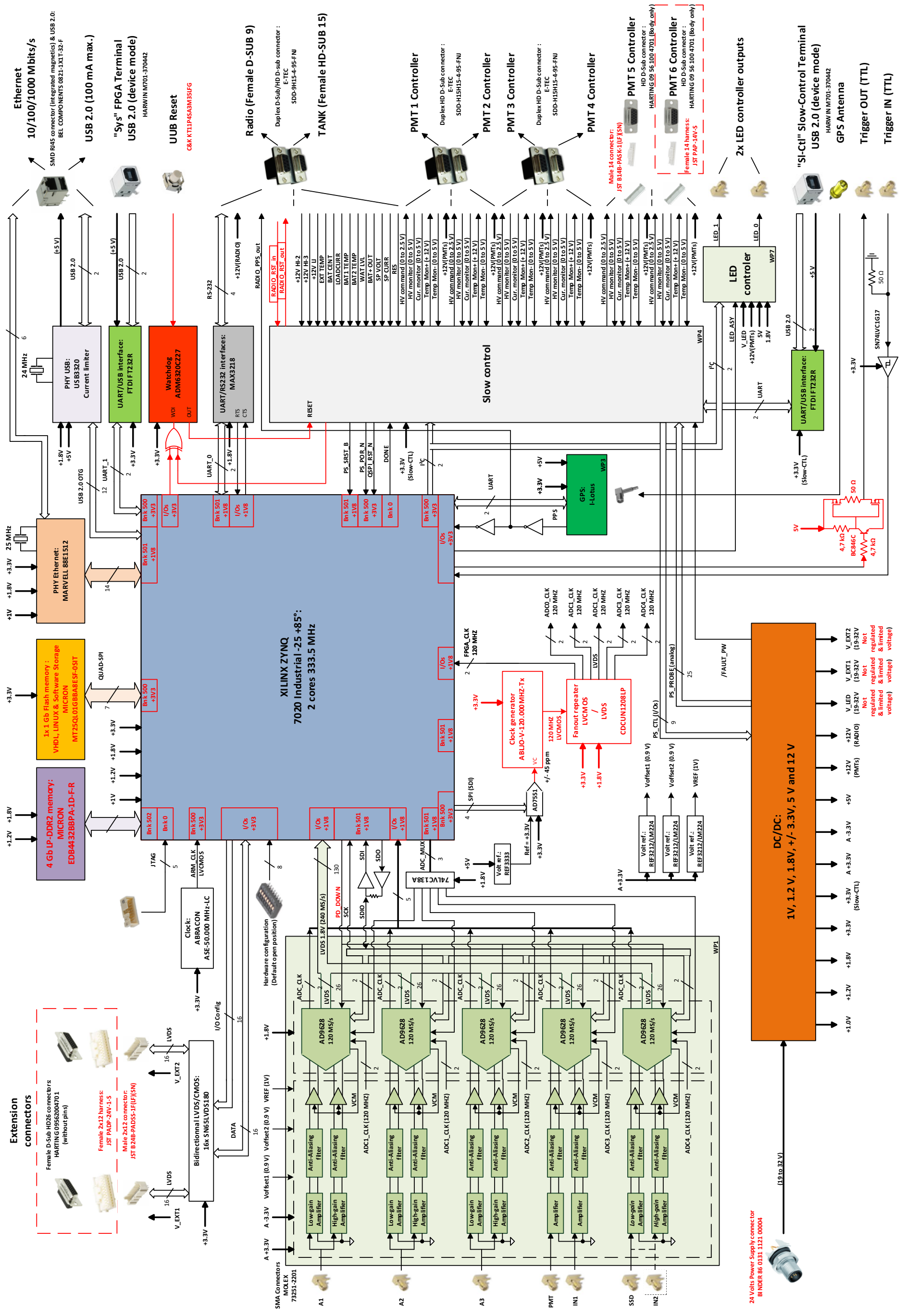

Figure 1: Upgraded unified board architecture.

5. Current status and performance

An engineering array with 12 AugerPrime prototype detector stations was deployed on the

Observatory site in October 2016. The data show generally good performance of the new electronics and satisfy most of the requirements. The noise levels are slightly higher than the requirements. However, the VEM and MIP calibration can be easily performed and the dynamic range is close to the requirements. The power consumption is currently 12 W which is higher than the 10 W requirement. The detectors have been continuously taking data since October without any problems due to the power system. The performances based on the first EA data are discussed in [3].

In order to further reduce noise, to lower the power consumption, and to implement some other minor changes, a new main electronics board has been designed. This board will be tested in laboratories and in the engineering array before the pre-production and production that are planned for early 2018.

6. Conclusions

The AugerPrime upgrade will complement the existing WCD with an additional SSD for better identification of air-shower particles. An extra small PMT will extend the dynamic range of the WCD. The upgraded Auger electronics will support the PMTs of the WCD and SSD detectors. It provides much higher performance in computing power, memory size, timing, and sampling frequency than the current electronics. Furthermore, the new electronics can be easily interfaced with any other additional detectors through the digital connectors.

Since October 2016, an AugerPrime engineering array has been in operation at the Auger Observatory site. The first results show generally good performance of the new electronics. To implement some minor design changes, a new main board is being fabricated and tested before the pre-production and production that are planned to start early 2018.

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