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3D Integration of Sensors and Electronics

R. Lipton*
Fermilab, Batavia, Illinois, USA
E-mail: lipton@fnal.gov

A three dimensional integrated circuit is composed of multiple tiers of integrated electronics and sensors integrated vertically by wafer bonding, thinning and insertion of through-silicon-vias. The technologies associated with three dimensional integrated circuits can provide new capabilities for high energy physics and x-ray imaging experiments. These include finer pixel pitch, lower interconnect capacitance, the ability to separate analog and digital functions, and better power distribution and connectivity. In this paper we review the status of 3DIC demonstration projects at Fermilab, discuss several possible applications, and summarize the current availability of commercial processes. Results of a three-tier demonstration project that includes designs for x-ray imaging, CMS track triggering, and ILC vertex are described. We discuss the status of several ongoing 3D projects and prospects for future evolution of the technology.

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*Speaker.

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1. The 3D Promise

A three dimensional integrated circuit is composed of two or more layers of active electronic components, integrated vertically by wafer bonding, thinning, and by insertion of through silicon vias (TSV) to connect layers. This is enabled by a suite of process technologies developed by industry over the past decade [1] [2] [3].

3D interconnect frees us from the design constraints imposed by traditional edge-based connections. Advantages include:

- Very fine pitch bonding. 1.5 micron pitch has been achieved with the DBI/Hybrid Bonding technique
- Much better power distribution and connectivity. The full surface area of the device is available for interconnects
- Radiation hard, thin sensors and readout. The process is radiation hard and thin sensors are readily accommodated
- Complex electronics without expensive process nodes. Multiple layers of large feature size nodes can replace expensive smaller nodes.
- Separation of analog and digital. This can provide better shielding and therefore lower thresholds.
- Lower interconnect capacitance. This can be a decisive advantage for faster, lower power devices operating in the picosecond range
- Tiled, large area devices. The combination of 3D and active or slim edge sensors can provide active tiles that can be deployed in large area sensors.

2. 3D Demonstration Project

We began exploration of 3D sensor/electronics integration in 2006 as it became clear that the very challenging requirements for low mass and high speed in ILC vertex detectors could not be achieved with technologies that were then available. At the time MIT-LL was developing a version of 3D integration based on their 180 nm SOI technology including detector thinning to 50 microns and backside laser annealing. We collaborated with MIT-LL in a DARPA-sponsored three-tier 3D run with the VIP, an ILC vertex chip with ADC, time stamp and sparse digitization [5]. This work continued with Cornell on backside contact formation on thinned detectors using laser annealing. We also undertook work with Ziptronix using their Direct Bond Interconnect (DBI) process to bond MIT-LL sensors to existing BTEV wafers and thin the sensors down to 100 microns [7].

Around 2009 Tezzaron, part of a 3D consortium with Ziptronix, had developed a 3D process that involved small ($\approx 1.2\mu m$) TSVs inserted at the initial phase of the wafer fabrication (via-first). Their process used direct bonds of the copper surface layers to provide inter-wafer contacts. Fermilab organized a multiproject run with a 17 member consortium to demonstrate this 3D process in the Chartered (now Global Foundries) 0.13 micron process. Fermilab contributed three designs; VIP, the ILC vertex chip; VICTR, a CMS track trigger front end chip; and VIPIC, a chip designed for x-ray correlation spectroscopy. The fabrication took about 18 months longer than anticipated, in part because the Tezzaron Cu-Cu bonding process was found not to be reliable. The Ziptonix DBI process was then tried and was successful.

2.1 DBI Hybrid bonding

The DBI process, also called "hybrid bonding" is now gaining broad acceptance in the semiconductor industry. Silicon tiers are connected using bonds between the top silicon dioxide layers with imbedded metal. The initial bond is at room temperature and can be reworked if necessary. The stack is then annealed at about 300 degrees to provide a strong, permanent bond and connect the imbedded copper [4]. This process can either be done using wafer-to-wafer bonding or chips can be bonded individually to wafers.

2.2 VIP, VICTR and VIPIC Results

After the initial two tier DBI bonding, wafers were sent to Ziptronix for chip-to-wafer bonding of the two CMOS layers to 500μm thick sensors fabricated at Brookhaven National Laboratory. This was a complex process with the top TSVs exposed and top metal patterned, a handle wafer attached, backside TSVs exposed and DBI layers applied. The wafers were then diced and the diced die were DBI bonded to the BNL sensor, the top handle wafer was then ground away and the top handle silicon etched to expose the contact metal pattern. The yield of good bonded die was about 60 percent.

A diagram and photograph of the resulting stack is shown in Figure 1. The contact pitch for the CMOS DBI layer was 3μm, the minimum pixel pitch (on the VIP) was 24μm and the total thickness of the two-tier CMOS stack with metal layers and silicon substrate was 34μm. All three 3D chips worked. The VIP and VICTR were tested on the bench. The VIPIC stack was extensively tested in particle and x-ray beams [10]. For the VIPIC x-ray imaging chip we were able to compare noise of the oxide-bonded pixels to the same chip with bump bonds to the sensor. The noise in the oxide bonded pixels is almost a factor of two lower than the conventionally bump bonded parts. This is due to the lower capacitance of the very small DBI interconnects and short routing paths compared to the 50 micron diameter bumps and associated pad capacitance.

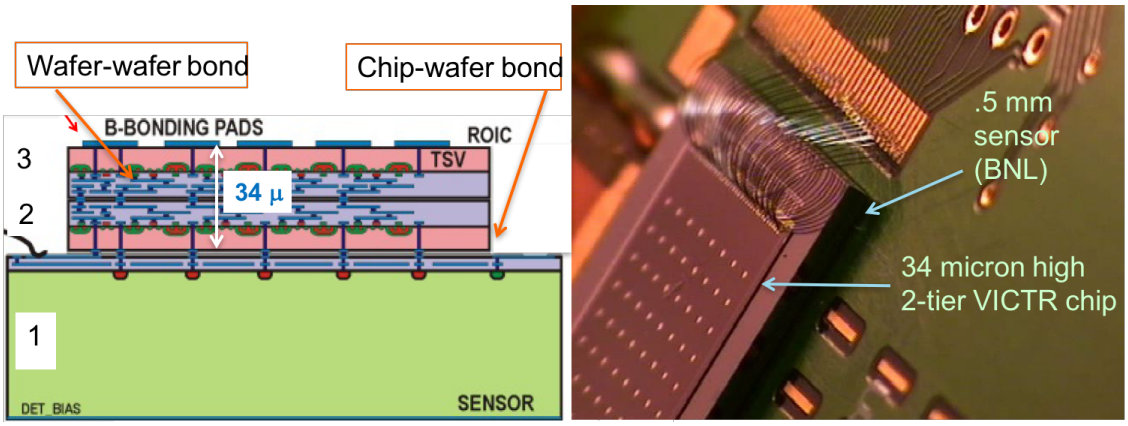

Figure 1: Left - Sketch of the two-tier 3D Stack. Right - Photograph of the VICTR stack mounted on a PC board.

3. Examples of Future Applications

There are several applications where 3D technology can significantly enhance the capabili-

ties of detector systems. We describe three examples below. There is also ongoing R&D on 3D SIPMs [12], 3D integration of monolithic active pixel sensors, and 3D integrated sensors for light sources [13].

3.1 Tiled Assemblies

There is a disparity between the ability to build large area silicon-based sensors of single 6" or 8" wafers and the limitation of Readout Integrated Circuit (ROIC) die to the 2×3 cm area of a typical CMOS reticule. The need to connect the ROIC both to the pixelated sensor contacts and external readout limits the ability to deploy large area arrays with minimal dead area. For example pixel detectors are typically assemblies of two columns of ROICs with wirebonded readout at the outside edges of the columns.

Three dimensional assemblies can solve these problems by providing connectivity both at the top and bottom of the ROIC stack. If we combine this technology with active-edge based sensors we can produce arrays of "active tiles" with minimal dead area and of arbitrary size. The basic unit is now a single reticule-sized sensor/ROIC stack. This stack can be individually tested and discarded if the sensor or ROIC is faulty. This avoids the multiplicative yield issues associated with wafer-scale bonded arrays. It also allows for cheaper, higher yielding, wafer-to-wafer 3D bonding as opposed to more difficult bonding of ROICs to large area sensor wafers.

We have a project underway to demonstrate the viability of this approach. Figure 2 shows the layout of the assembly. The sensor is fabricated on a 6" SOI stack with a 500 micron bottom "handle" wafer oxide bonded to a 200 micron float zone sensor tier fabricated by VTT. The sensor has been fabricated using an active edge process which utilizes trenches filled with doped polysilicon to provide the doping for the active edge. This sensor stack is then planarized and hybrid bonded by Ziptronix to a top wafer which contains aluminum routing layers intended to simulate a ROIC. These traces route the sensor strips to contact locations on the bottom layer of the dummy ROIC. When the dummy ROIC is bonded to the sensor wafer these pads are now on the top (silicon-facing) surface. The dummy ROIC silicon is then ground down to a total thickness of 10 microns. Silicon is then etched away to the dummy ROIC contact locations and a redistribution aluminum layer is deposited to route signals to the bump bond pads.

The bonded wafers have been tested and perform as expected. The final process of dicing is now underway using a laser to retrench the wafers to a depth of 250 microns. These will then be ground from the backside to singulate the die for incorporation into test devices.

3.2 Fast Timing

The time resolution due to noise-related jitter for a device with a constant voltage threshold can be expressed as

$$\sigma_t \sim \tau_{rise}\left(\frac{Noise}{Signal}\right),\ \sigma_t \sim \frac{\sigma_n}{\frac{\partial V}{\partial t}}(constant signal) \tag{3.1}$$

$$\sigma_n^2 = \frac{C_L^2(4kTA)}{g_m t_a},\ \sigma_t \sim \frac{C_L}{\sqrt{g_m t_a}}\sqrt{t_a^2 + t_d^2} \tag{3.2}$$

Where C_L is the detector load capacitor, g_m is the front end amplifier transductance, and $t_a \sim \frac{\partial V}{\partial t}$ and t_d are the rise times of the amplifier and detector. Crucial factors for time resolution are the rise

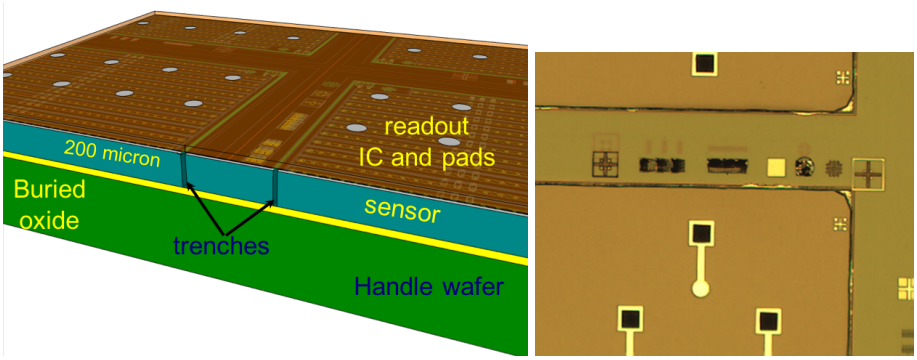

Figure 2: Left - Drawing of the active edge demonstration wafer. The sensor is 200 micron thick float zone SOI bonded to a 500 micron thick handle wafer. The active edge is composed of 50 micron wide polysilicon-filled trenches that provide doping of the sensor edge. This sensor contains a pattern of short strips. Right - Picture of the trenched region between two sensors showing the through silicon connection (dark squares) and associated bump bond redistribution traces.

times of the amplifier/detector system and the signal to noise of the system, which in turn depends on the load capacitance. LGAD-based systems attack the problem by using avalanche gain to increase the signal by a factor of ≈ 10. A 3-D integrated system has the potential to significantly decrease the noise by lowering the load capacitance. This is possible due to the very fine pitch capability and by the inherently low interconnect capacitance of the hybrid/DBI bond. This was demonstrated in the VIPIC-1 [10] discussed in section 2.2. We have measured TSV capacitance of about 8 ff in VIPIC-L test devices. TCAD simulations show the capacitance of the sensor for a 50 micron thick 33 micron pitch sensor pixel to be about 7 ff. Thus it is likely that the total load capacitance can be kept below 25 ff, to be compared with ~ 2 pf for the typical 1 mm pixel associated with LGADs, 80 times smaller. Of course there are many more pixels per unit area in the small pixel sensor, and therefore potentially more total power in the front end amplifiers and associated downstream electronics. As shown in in equation 3.2, signal/noise is a function of $\sqrt{g_m}$ (which, in turn, depends on the associated front-end current) and is linear in capacitance. This means that the front end current per pixel can be considerably reduced while preserving excellent time resolution and adding the benefit of excellent spatial resolution. These tradeoffs would need to be studied in detail for a specific application.

3.3 High Energy X-rays

With the continued expansion of light sources there has been a parallel growth of applications for pixel detectors in x-ray imaging. Some of these applications also require sub-nanosecond timing. In this case there are competing needs for efficient detector of high energy x-rays, which requires thick silicon detectors, and fast timing, which is generally considered to require thin detectors. A 3D pixelated detector could resolve these competing requirements. The shape of a current pulse detected by an amplifier connected to a pixel is determined by a combination of the magnitude and velocity of the charge cloud moving in the detector's electric field and the weighting field associated with the particular geometry of electrodes [11]. In a detector where the pixel pitch is small compared to the thickness of the sensor the induced current in an electrode far from the

moving charge cloud is very different than the induced current due to charge close to the collection electrode. Far from the pickup electrode (*thickness* >> *pitch*), the shapes of the initial parts of the current pulses are similar, with differences developing as the charge cloud drifts toward the electrode surface.

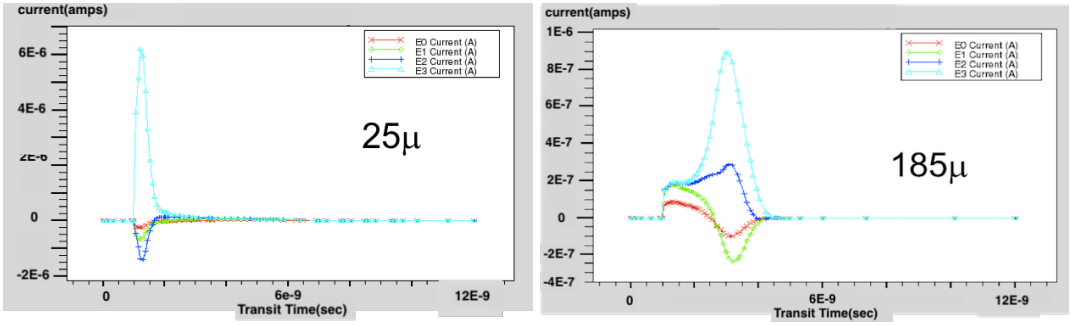

Figure 3: Left - Pulse shapes of central and neighboring pixels for an x-ray deposited 25μ below the surface of a 200 micron thick detector with 33μ pitch. Right - Pulse shapes for an x-ray deposited at 185μ. Blue, green, and red traces are neighbor, next neighbor, and third neighbor pixels

An example is shown in Figure 3 . X-rays converted near the surface produce a large, clean pulse in the central pixel. X-rays deposited deep in the sensor produce a delayed pulse in the central pixel and fast rise, bipolar pulses in the neighboring pixels. In this situation, with fast amplifiers in each pixel, a conversion deep in the silicon can contribute many time stamps (perhaps 8-16). Each of these time stamps would have poorer resolution than the single large pulse, but the information can be combined in an upper tier of readout electronics that can process a field of pixels. Such an intelligent sensor could then use all of the information from the local region to determine the time of arrival, position, and conversion depth of a high energy x-ray.

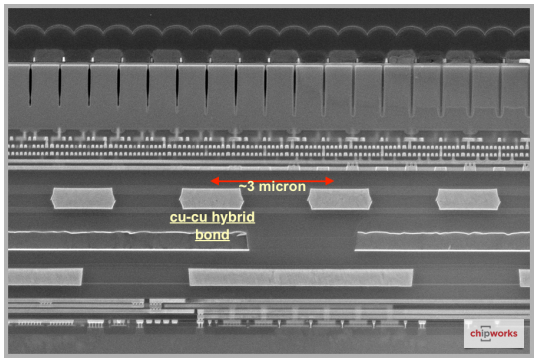

Figure 4: Section of the Sony Exmor camera chip showing the hybrid bond interface (Chipworks)

4. Availability and Cost

Microelectronics is a very cost-sensitive industry. Technologies which are technically appealing often fail due to lack of industrial support, standardization, or most important, cost. MCM-D - thin film on silicon - is an example. It appears that 3D has survived the shake-out process and

has become a mainstream technology, with wide application in image sensors. The DBI/Hybrid bonding technology developed by Ziptronix and which we began exploring in 2008 now appears to be the process of choice. For example, hybrid bonding is now used by Sony in the Iphone 8 and X cameras. For particle physics, we need to find vendors willing to work on the small scale represented by scientific applications and with the technical capability to deliver reliable devices for projects. The range of vendors providing hybrid bonding services has expanded significantly in the last year. A partial list of vendors providing or developing hybrid bonding includes Sony, SMIC, Nhanced/Scorpious, Teledyne Dalsa, IZM, Raytheon, Sandia lab and MIT-Lincoln Labs. Some offer only wafer-to wafer processes, while others also provide die-to wafer options. Associated processes, such as wafer thinning and through silicon via insertion, are typically available, with varying via size and wafer thickness capabilities. Costs remain a concern, but with the more widespread availability of the processes costs are likely to drop. Applications that can use a single readout chip layer can avoid the expense of small TSVs and build single hybrid bonded layers with large dimension topside contacts as we used in the active edge demonstrator.

In addition to the 3D hybrid bonding described above, 2.5D "interposer" structures, which utilize TSV-based technologies, can be used as micro circuit boards with trace pitches an order of magnitude smaller then conventional printed circuit boards [14]. Interposers can provide a circuit layer with a level of integration intermediate between integrated circuits and PC boards. These can be fabricated with silicon, glass or organic substates. Glass is of particular interest because of it's low dielectric constant. Interposers can provide sensor to readout chip pitch adapters, house very high speed interconnects between active die and integrate passive components.

5. Conclusions

Over the last several years multiple hybrid bonding vendors have emerged and there is now access to multiple 3D processes with or without fine TSVs, several at the scale appropriate to scientific applications. The question is no longer if 3DIC technology is commercially viable, but how the new technologies can best serve our needs. These technologies can offer a combination of very low interconnect capacitance, separation of analog and digital, access to very fine pitch pixels, and new geometrical options for sensor/readout interconnect. 3D stacking can be used in combination with CMOS MAPS to provide an optimal combined design with digital tiers separated from analog, logic viewing a field of pixels, or mixed IC technology nodes. Associated 2.5D interposer technologies can provide techniques to optimally match sensor and readout system geometries.

As designers and developers of scientific instrumentation, we constantly seek to utilize an optimal mix of technologies. A detector for a small e^+e^- vertex detector may be very different from a large area tracking detector for LHC or a focal plane for X-ray imaging. The optimization must involve physics requirements, sensor performance, electronics capabilities, and overall cost. We are constantly asked to meet challenges in areas such as speed, intelligent correlation of information, and sensor geometries, coming from the drive to extend our physics reach. 3D integration provides a compelling set of capabilities that can be used to help meet these new challenges.

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