

## Development of Silicon-on-Insulator Pixel Devices

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Development and application of Silicon-on-Insulator (SOI) monolithic pixel devices has been significantly boosted in recent years. After a brief review of the recent SOI development activities in various sciences, we detail the test-beam results achieving a sub-micron spatial resolution, 0.65  $\mu\text{m}$ , first time by a semi-conductor device, with Fine-Pixel Detector (FPIX) which has a pixel size of  $8 \times 8 \mu\text{m}$  pixel size and thickness of 500  $\mu\text{m}$ . Another device SOFIST with pixels of  $20 \times 20 \mu\text{m}$  and thickness of 500  $\mu\text{m}$  showed a spatial resolution of  $\sim 1.2 \mu\text{m}$ . Thinner devices as required for the ILC experiment are expected to be an excellent candidate even with reduced signal-to-noise ratio.

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## 1. Introduction

Monolithic semiconductor pixel devices are attractive for particle detector application in various aspects. They are not subjected to the same geometric manufacturing constraints as hybrid pixel devices, e.g., metal bumps which limit their pixel size typically to 50  $\mu\text{m}$  [1]. Under the supports provided by the five-year JSPS Grant-in-Aid “Interdisciplinary research of quantum imaging opened with 3D semiconductor detector” [2], we have been developing fully depleted silicon-on-insulator (FD-SOI) monolithic pixel devices that utilize the Lapis 0.20- $\mu\text{m}$  technology [3].

The SOI precision particle detectors have been realized through various improvements adopted in the SOI technology. The major three issues were: suppression of the back-gate effect, suppression of the cross-talk, and improvement of radiation hardness. Introduction of a buried p-well (BPW), which is typically tied to a p-type pixel node for n-type substrates, successfully suppresses the back-gate effect by shielding the electric field from the back-bias [4], [5]. The remaining two issues were overcome by innovating double-SOI wafers [6]. The second active Si layer is used as shielding against the cross-talk between the pixel node to near-by electronics [7], and as the negative-potential electrode to compensate the effect of holes in the insulator accumulated as total ionization dose (TID) effect [8].

In Sec. 2, we briefly summarize the status of the double SOI wafers (DSOI) and typical project progresses in the SOI pixel development. One of the device R&D targets we set in conducting the grant-in-aid research is to realize a detector with sub-micron spatial resolution. A fine-pixel detector (FPIX) has been designed to demonstrate the excellent spatial resolution achievable with the SOI monolithic pixel [9]. We also began to develop a pixel detector dubbed the SOI sensor for Fine measurement of Space and Time (SOFIST) [10] for the ILC experiment [11] which took full advantage of the FD-SOI device characteristics. Section 3 reviews the designs of the FPIX and SOFIST, and their testbeam setup conducted at the FNAL Test beam facility (FTBF). The spatial resolution results are given in Sec. 4, then followed are summary and prospects.

## 2. DSOI and SOI Projects

The DSOI wafers are fabricated by repeating twice the SmartCut™ process developed by Soitec [12]. Table 1 summarizes the main parameters of the DSOI wafers. D-3 is adopted in the on-going MPW process, where the substrate resistivity is significantly increased by introduction of FZ wafers by Shin-Etsu Chemical Co., Ltd. The wafers are in 8 inches and 725  $\mu\text{m}$  in thickness, which are thinned to 300  $\mu\text{m}$  by Lapis. Further thinning down to 50  $\mu\text{m}$  is possible by other commercial process.

TABLE 1. Main parameters of the double SOI wafers. (SOI: active silicon, BOX: buried oxide)

Layer	D-1 (SOITEC)	D-2 (Shin-Etsu)	D-3 (Shin-Etsu)
SOI1	p-type 88nm thick, $\rho < 10\Omega\text{cm}$		
BOX1	145 nm thick		
SOI2	p-type 88nm, $< 10\Omega\text{cm}$	n-type 150nm, $< 10\Omega\text{cm}$	n-type 150nm, 3-5 $\Omega\text{cm}$
BOX2	145 nm thick		
substrate	n-type, CZ $> 700\Omega\text{cm}$	p-type, lowO <sub>2</sub> CZ $> 1.0\text{k}\Omega\text{cm}$	p-type, FZ $> 5.0\text{k}\Omega\text{cm}$

Table 2 is a brief summary of typical SOI applications. Among these, the DSOI has improved substantially the performance of XRPIX and CNTPIX where on-pixel digital signaling is required. FD-SOI FETs exclusively work at cryogenic temperatures and two projects utilize SOI for implementing the readout electronics.

TABLE 2. Typical SOI sensor applications.

Sensor	Description (typical applications)
INTPIX	Integration type. Latest is INTPIX8. Active area: $8.7 \times 14.1 \text{ mm}^2$ with $12 \times 12 \mu\text{m}$ pixels [13](Strain measurement using X-rays and Readout for pulse TEM)
SOPHIAS	For synchrotron radiation at SACLA RIKEN. Active area: $64.8 \times 26.7 \text{ mm}^2$ with $30 \times 30 \mu\text{m}$ pixels. Frame rate: 60 Hz.[14]
XRPIX	Satellite cosmic X-rays with self-trigger function. Active area: $8.7 \times 14.1 \text{ mm}^2$ Noise $10e^-$ (rms). Frame rate: 100 kHz.[15]
cryogenic	SOI works exclusively at cryogenic temperature. (R/O for superconducting tunneling junction detector STJPIX [16] and R/O for far infrared detector[17])
CNTPIX	Counting type with hexagonal pixels at $52 \mu\text{m}$ spacing. 19-bit counter, 7-bit register and charge-share handling logics on each pixel [7]
MALPIX	For mass-spectroscopy of laser-dissociated ions operated with MCP in front. Active area: $25.6 \times 25.6 \text{ mm}$ . $512 \times 512$ pixels

### 3. FPIX and SOFIST for FNAL Testbeam

The FPIX2 [18], a family of INTPIX eliminating storage on-pixel capacitors (see Fig. 1), has a  $128 \times 128$  matrix of  $8 \times 8 \mu\text{m}$  pixels, comprising an  $1 \times 1 \text{ mm}$  active area set in a chip size of  $2.9 \times 2.9 \text{ mm}$ . The signals are extracted in rolling-shutter mode and digitized by external 12-bit ADCs set in a SEABAS2 board [19]. There are eight parallel readout lines, thus each ADC handles signals of 16 (of the 128) columns  $\times$  128 rows. The scan time was 280 ns to allow each signal to be digitized by the ADC at a frame rate of 1 kHz. The tested chips are with FZ p-type substrates of  $20 \text{ k}\Omega\text{cm}$  and  $500 \mu\text{m}$  thickness.

The SOFIST-v1 [10][20] is also an integration type of  $20 \times 20 \mu\text{m}$  pixels implemented with two on-pixel analog memories (Fig. 1). The on-pixel comparator/shift register switches the memories to deal with multiple hits before the memories are read out. The signals are digitized either by 8-bit ADCs implemented in each column end or by 12-bit ADCs of the SEABAS2. The tested chips are with sensitive area of  $1 \times 1 \text{ mm}$ , FZ n-type substrates of  $2 \text{ k}\Omega\text{cm}$  and  $500 \mu\text{m}$  thickness.

We evaluated the tracking performance of four FPIX2 and two SOFITSv1 subjected to a 120 GeV proton beam at FNAL, as illustrated in Fig. 1. The digitized signals stored in six SEABAS2 boards are read out upon receiving a trigger generated from a scintillation counter  $3 \times 3 \text{ mm}$  and an ATLAS pixel detector with an FE-I4 readout chip [16] defining a Region-of-Interest area of  $1.5 \text{ mm}$  square. Further description of the setup, hit clustering and tracking are detailed in [18].

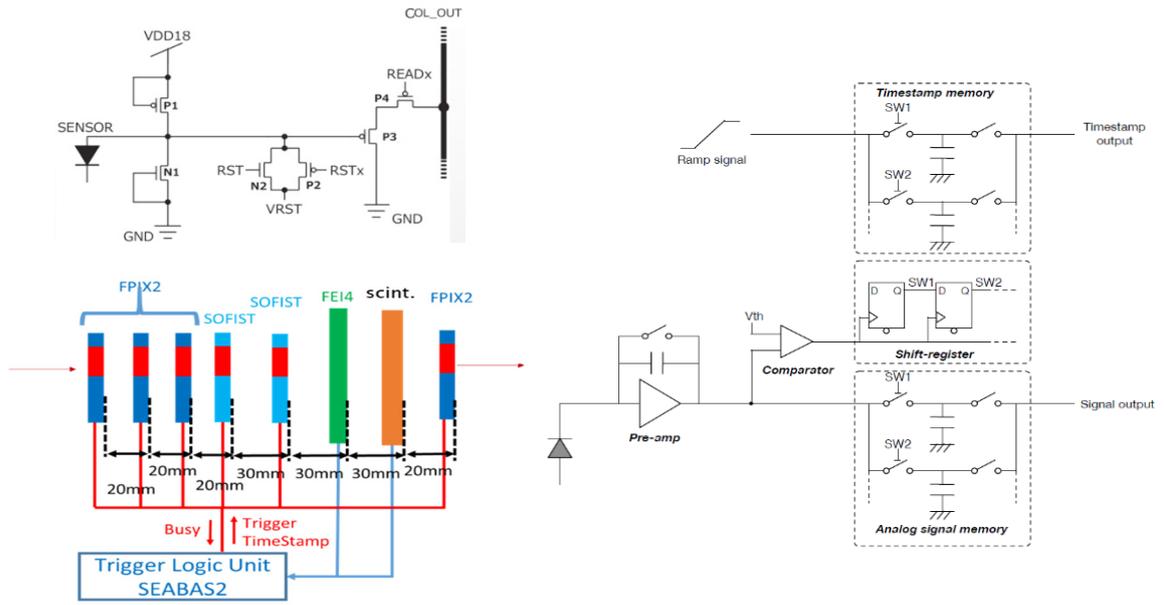


Fig. 1. (Top-left) FPIX2 on-chip circuit, (right) SOFIST on-chip circuit. The timestamp memory section is not included in SOFIST-v1. (Bottom-left) Setup at FNAL test beam facility showing the relative positions of the detectors along the beam direction.

#### 4. Results of Spatial Resolution

##### 4.1 FPIX2 spatial resolution

In Fig. 2, the residuals are plotted as a function of the global track position reconstructed using the three FPIXs other than the one under investigation, FPIX2-2 or FPIX2-3 in these plots. The hit positions are simply the average position weighted by the charge and the track is a fit to a simple straight line. The rms spreads are affected by imperfect detector alignment as indicated. Restricting the range of the global position results in more uniform resolutions values among the four FPIX2s as compared to the previous results [18] where no restriction was applied in evaluating the resolutions. Figures 3 shows the horizontal (X) residual distributions to the global track. The observed residual spreads differ reflecting the different relative Z positions along the beam. The poor residuals of the last FPIX2 plane, for example, are due its location at a rather large distance from the other three planes, and after the material of other devices along the beam. Similar plots of the vertical (Y) coordinate are shown in Fig.4.

**TABLE 3.** Measured FPIX2 residual spread and evaluated intrinsic resolution. Units:  $\mu\text{m}$ .

	1X	2X	3X	4X
Meas. residual	0.953±0.009	0.791±0.008	0.822±0.008	3.80±0.05
Intrinsic resolution	0.711±0.009	0.648±0.008	0.703±0.008	0.75±0.01
	1Y	2Y	3Y	4Y
Meas. residual	0.833±0.008	0.683±0.006	0.824±0.008	3.79±0.05
Intrinsic resolution	0.622±0.008	0.600±0.006	0.704±0.008	0.75±0.01

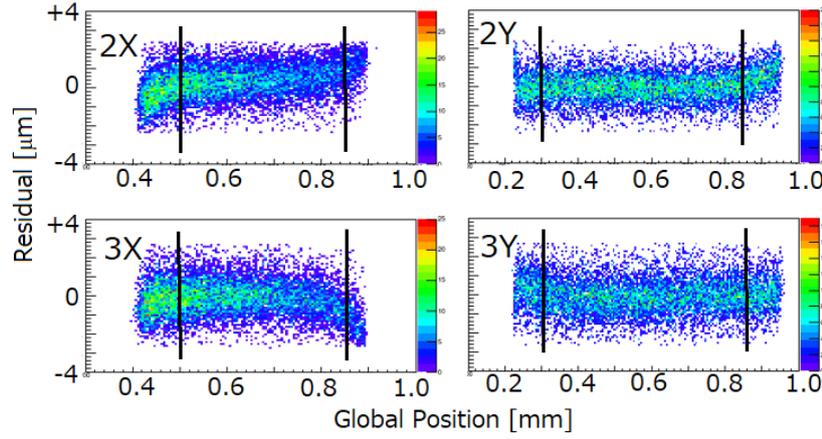


Fig. 2. Residuals in the four coordinates, 2X, 2Y, 3X and 3Y, as a function of the global track position. The data samples within the two vertical lines are used for Fig. 3 and Fig. 4.

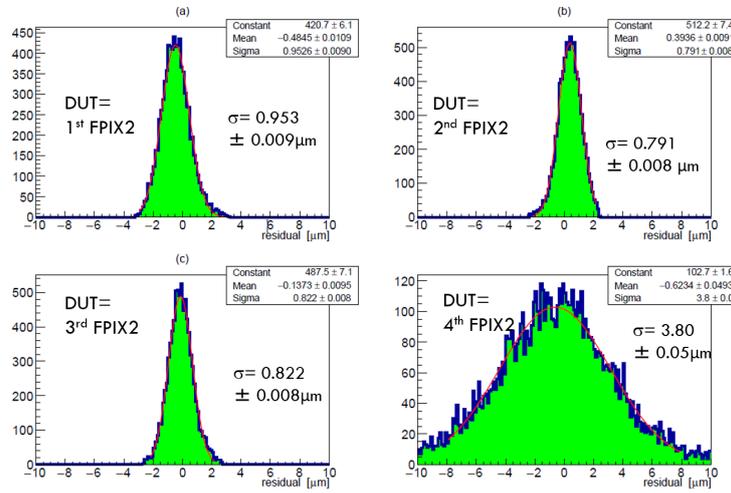


Fig. 3. Residual distributions in horizontal direction to the track reconstructed using the three FPIXs other than the one under investigation for (a) 1<sup>st</sup> FPIX, (b) 2<sup>nd</sup> FPIX, (c) 3<sup>rd</sup> FPIX and (d) 4<sup>th</sup> FPIX. X-axis is in micrometers

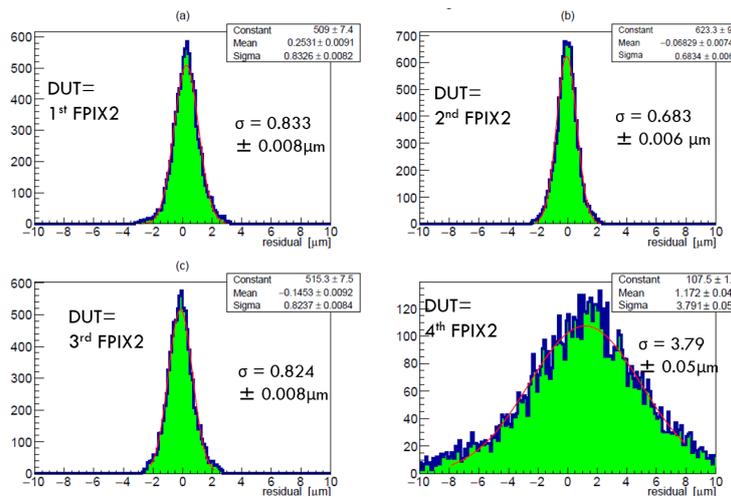


Fig. 4. Residual distributions in vertical direction to the track reconstructed using the three FPIXs other than the one under investigation for (a) 1<sup>st</sup> FPIX, (b) 2<sup>nd</sup> FPIX, (c) 3<sup>rd</sup> FPIX and (d) 4<sup>th</sup> FPIX. X-axis is in micrometers

As the measured residual spreads can be assumed as a quadrature sum of the intrinsic spatial resolution and the track uncertainty, we estimated the intrinsic resolution by assuming that the four FPIXs have the same intrinsic resolution. Under this assumption, the track uncertainty at specific Z position can be analytically given<sup>2</sup> in term of the intrinsic resolution and the geometrical Z positions of the detectors. The correction factors ( $\sigma_{\text{meas}}/\sigma_{\text{intr}}$ ) are 1.34, 1.22, 1.17 and 5.08 for the cases where the 1<sup>st</sup> to 4<sup>th</sup> FPIXs, respectively, are under evaluation. The measured residual sigma and extracted intrinsic resolution are summarized in Table 3.

## 4.2 SOFIST-v2 spatial resolution

Figure 5 shows the Y residual distributions for the two SOFIST-v1 sensors against the tracks reconstructed by the four FPIX2 sensors. The spatial resolution has been examined for the three conditions: (1) 500  $\mu\text{m}$  full depletion (at 500 V bias) readout by external 12-bit ADC, (2) 200  $\mu\text{m}$  partial depletion (at 15 V bias) readout by external 12-bit ADC, and (3) 500  $\mu\text{m}$  full depletion readout by column 8-bit ADC. The obtained three rms values are shown in the figure.

The uncertainties of the FPIX2 tracks at the positions of SOFIST1 and 2 are 0.57 and 0.65  $\mu\text{m}$ , respectively, for the FPIX2 intrinsic resolution assigned as 0.65  $\mu\text{m}$ . The residual spread subtracted with them in quadrature are summarized in Table 4. The signal-to-noise ratio (S/N) is around 300 for condition (1) and 120 for condition (2) [20]. The S/N for condition (3) was not extracted reliably for the 8-bit ADC resolution.

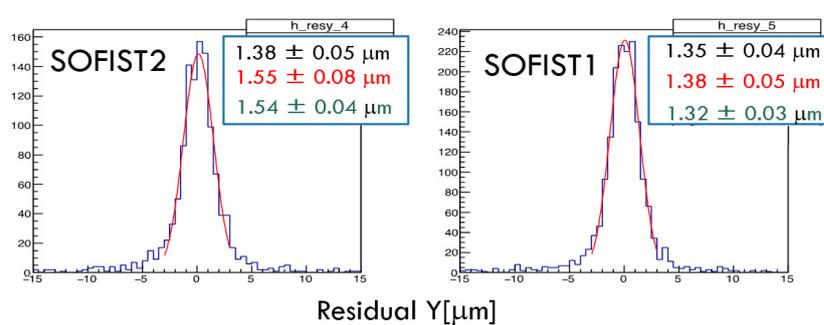


Fig. 5. Residual distributions in Y coordinate for the two SOFIST-v1 sensors. The three values are rms spreads of distributions for the three conditions, while the distributions are for the condition (1), see text.

**TABLE 4.** SOFIST residual spread with FPIX2 track uncertainty subtracted. Units:  $\mu\text{m}$ .

	SOFIST1 X	SOFIST1 Y	SOFIST2 X	SOFIST2 Y
Condition (1) S/N~300	1.23±0.04	1.22±0.04	1.35±0.05	1.22±0.05
Condition (2) S/N~120	1.38±0.06	1.26±0.05	1.46±0.08	1.41±0.08
Condition (3)	1.20±0.03	1.19±0.03	1.44±0.06	1.40±0.04

<sup>2</sup> The global track parameters are determined by a least-square fit to the three hit positions other than the DUT (detector under test). As the track parameters can then be expressed in analytical forms, their uncertainties, hence the uncertainty at a specific Z position (at the DUT) is given by the spatial resolutions of the individual tracking planes. Here we assume that the individual resolutions are same  $\sigma_{\text{intr}}$ , the measured resolution  $\sigma_{\text{meas}}$  is simply a function of  $\sigma_{\text{intr}}$ ,  $\sigma_{\text{meas}}^2 = (\kappa_1 + \kappa_2 + \kappa_3)\sigma_{\text{intr}}^2$ , where  $\kappa_i$ 's are the weight factors determined by the relative Z positions of the three tracking planes. The effect of residual mis-alignment and multiple scattering  $\sigma_{\text{other}}$  may modify the relation as  $\sigma_{\text{meas}}^2 = (\kappa_1 + \kappa_2 + \kappa_3)\sigma_{\text{intr}}^2 + \sigma_{\text{other}}^2$ , therefore neglecting  $\sigma_{\text{other}}$  results in a conservative estimate on  $\sigma_{\text{intr}}$ .

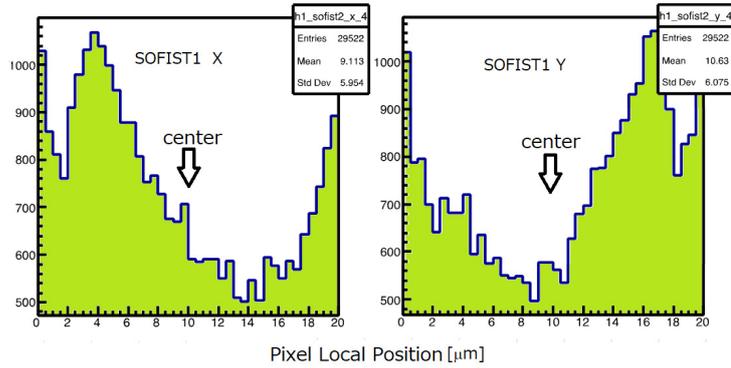


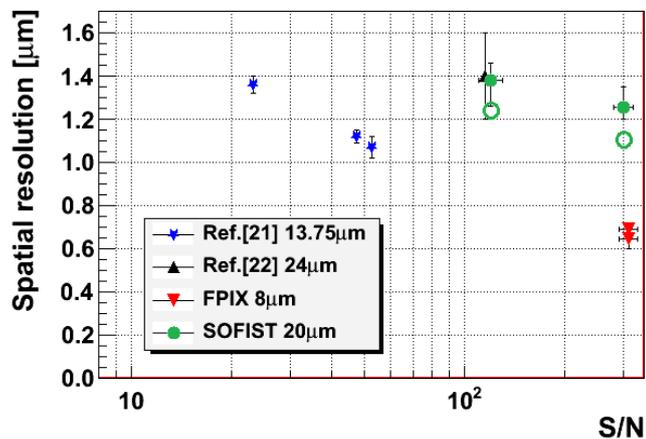
Fig. 6. Event populations within the pixel for SOFIST1 (left) X and (right) Y for the condition (1). The pixel center is located at position of 10  $\mu\text{m}$  and the pixel is 20  $\mu\text{m}$  wide. The vertical is the number of events (zero suppressed).

For the condition (1), an average of 1.26  $\mu\text{m}$  is obtained for the resolution subtracted with the FPIX2 track uncertainty. Figure 6 shows the event population within the pixel as a function of the local pixel coordinate with the pixel center located at 10  $\mu\text{m}$  and boundaries at 0 and 20  $\mu\text{m}$ . The structures are observed similar for the two SOFISTs independently with respect to the global position, but differently in X and Y coordinates, as shown. As the event population is expected to be flat, the observed structures can be used to correct for the deviations caused by the hit point calculation. The rms deviation of the charge-weighted position to the position to flatten the population was found typically 0.6  $\mu\text{m}$ . The obtained 1.26  $\mu\text{m}$  is thus expected to be reduced to 1.10  $\mu\text{m}$  by applying this correction (so called  $\eta$  correction). The observed asymmetry about the pixel center should be explained by non-uniform charge collection. Further systematic study including understanding of the cause for the asymmetry is in progress.

### 4.3 Comparison with previous work

Previous devices developed under the constraint of achieving a resolution close to 1  $\mu\text{m}$  can be found in [21] and [22]. Figure 7 compares their spatial resolutions with the present values as a function of S/N. The FPIX2 data points are shown separately for the X and Y coordinate values with averages of 1<sup>st</sup> to 3<sup>rd</sup> FPIX2 sensors taken as the central values and the differences from the maximum and minimum values indicated by the error bars. Averages of SOFIST data are shown for the conditions (1) and (2), separately.

Fig. 7. Comparison of the spatial resolutions with that in previous works. S/N is calculated as the cluster charge divided by single pixel noise. Ref. [21] uses the average charge (typically 10% larger than MPV charge) for the signal S, while the others use the MPV charge. For SOFIST, the data points shown in filled circles are for the resolution with the reference track uncertainty subtracted. Possible improvements by correcting for biased position calculation due to simple charge weighted mean are shown in open circles. The pixel sizes are shown in the figure.



The approximate agreement seems between the results of [21] and FPIX, and the results of [22] and SOFIST is the result of the similarity in pixel pitch. The sets of data points lie on a roughly straight line on a log scale, which implies a rather pronounced deviation from the simple relation  $\sigma \propto \frac{1}{S/N}$  between resolution  $\sigma$  and S/N ratio.

## 5. Summary and prospects

The SOI's five-year grant-in-aid research is ending. One of the project targets to achieve sub-micron spatial resolution has been successfully realized, achieving 0.65  $\mu\text{m}$  by FPIX having pixels of  $8 \times 8 \mu\text{m}$ . A spatial resolution of  $\sim 1.2 \mu\text{m}$  is expected for the SOFIST having pixels of  $20 \times 20 \mu\text{m}$ . Although the obtained SOFIST spatial resolution sufficiently meets the requirement for the ILC experiment, such devices as thick as 500  $\mu\text{m}$  clearly do not meet the requirement on the material budget. Devices of 100  $\mu\text{m}$  thickness seem to be an excellent ILC candidate.

We continue to evaluate the time-stamp function which has been implemented in SOFIST-v2. SOFIST-v3 with both v1 and v2 functions implemented in pixels of  $30 \times 30 \mu\text{m}$  is under the current Lapis process. SOFIST-v4 is also under the process to investigate 3D stacking. One chip having preamplifier/discriminator and another chip having shift-register/3-analog and 3-time-stamp memories will be stacked using cone-shaped micro Au bumps [23]. Four 4.5- $\mu\text{m}$  high bumps will connect upper and lower chip circuits per pixel of  $20 \times 20 \mu\text{m}$ .

Many fruitful outcomes and progresses achieved in the grant-in-aid research framework ensure us wider application possibilities of the SOI pixel technology for new sciences, and encourage us to continue further enhancement of the SOI technology.

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## References

- [1] G. Aad *et al.*, J. Instruments 3 P07007 (2008).
- [2] [http://soipix.jp/index\\_en.html](http://soipix.jp/index_en.html).
- [3] Lapis Semiconductor Co., Ltd., <http://www.lapis-semi.com/en/>.
- [4] Y. Arai *et al.*, Nucl. Instr. Meth. A636, S31 (2011).
- [5] M. Kochiyama *et al.*, Nucl. Instr. Meth. A636, S62 (2011).
- [6] M. Okihara *et al.*, "Lapis SOI Pixel Process", talk given at Int. Workshop on SOI Pixel Detector (SOPIX2015), Sendai, Japan, June (2015): arXiv:1511.05224 [physics.ins-det].

- [7] Y. Lu *et al.*, "An SOI pixel sensor with in-pixel binary counters", talk given at Int. Conf. on Technology and Instrumentation in Particle Physics (TIPP'17), May 22-26, 2017, Beijing, China.
- [8] S. Honda *et al.*, Proc. Of Sciences, PoS (TIPP2014) 039.
- [9] Hara, K. *et al.*, "Development of Fine Pixel Detector for HEP Experiments Based on Innovative Double SOI Technology", talk given at IEEE&MIC, San Diego, USA on Nov. 4 (2015).
- [10] S. Ono *et al.*, "A monolithic pixel sensor with fine space-time resolution based on Silicon-on-Insulator technology for the ILC vertex detector", talk given at Int. Conf. on Technology and Instrumentation in Particle Physics (TIPP'17), May 22-26, 2017, Beijing, China.
- [11] ILC Technical Design Report 2013: <https://www.linearcollider.org/ILC/Publications/Technical-Design-Report>.
- [12] Soitec, <https://www.soitec.com/en/products/smart-cut>.
- [13] T. Miyoshi *et al.*, "Performance study of double SOI image sensors", talk given at 19<sup>th</sup> Int. Workshop on Radiation Imaging Detectors (iWoRiD 2017), July 2-6, 2017, Krakow, Poland.
- [14] T. Hatsui *et al.*, "SOPHIAS for the X-ray Free-Electron laser Experiments", talk given at 10<sup>th</sup> Int. Meeting on Front-End Electronics (FEE 2016), May 30-June 3, 2016, Krakow, Poland.
- [15] S. Ohmura *et al.*, "Reduction of cross-talks between circuit and sensor layer in the Kyoto's X-ray astronomy SOI pixel sensors with double-SOI wafer", NIM A831, 61 (2016).
- [16] S. Kim *et al.*, "Development of Superconducting Tunnel Junction Photon Detector with Cryogenic Preamplifier for COBAND experiment", talk given at Int. Conf. on Technology and Instrumentation in Particle Physics (TIPP'17), May 22-26, 2017, Beijing, China.
- [17] T. Wada *et al.*, "Development for Germanium Blocked Impurity Band Far-Infrared Image Sensors with Fully-Depleted Silicon-On-Insulator CMOS Readout Integrated Circuit", J. of Low Temp. Phys., 184, 224 (2016).
- [18] K. Hara *et al.*, "Fine-pixel detector FPIX realizing sub-micron spatial resolution developed based on FD-SOI technology", talk given at Int. Conf. on Technology and Instrumentation in Particle Physics (TIPP'17), May 22-26, 2017, Beijing, China.
- [19] R. Nishimura *et al.*, "DAQ Development for Silicon-On-Insulator Pixel Detectors", talk given at Int. Workshop on TSOI Pixel Detector (SOIPIX2015), June 3-6, 2015, Sendai, Japan; arXiv:1507.04946v1.
- [20] M. Yamada *et al.*, "Development of monolithic pixel detector with SOI technology for the ILC vertex detector", talk given at 19<sup>th</sup> Int. Workshop on Radiation Imaging Detectors (iWoRiD 2017), July 2-6, 2017, Krakow, Poland.
- [21] M. Battaglia *et al.*, Nucl. Instr. Meth. A676, p50 (2010).
- [22] M. Boronat *et al.*, IEEE TNS 62-1, p381 (2015).
- [23] F. Imura *et al.*, Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th, pp1915 -1920 (2014).