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CBC3: a CMS microstrip readout ASIC with logic for track-trigger modules at HL-LHC

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The CBC3 is the latest version of the CMS Binary Chip ASIC for readout of the outer radial region of the upgraded CMS Tracker at HL-LHC. This 254-channel, 130nm CMOS ASIC is designed to be bump-bonded to a substrate to which sensors will be wire-bonded. It will instrument double-layer 2S-modules, consisting of two overlaid silicon microstrip sensors with aligned microstrips. On-chip logic identifies first level trigger primitives from high transverse-momentum tracks by selecting correlated hits in the two sensors. Delivered in late 2016, the CBC3 has been under test for several months, including X-ray irradiations and SEU testing. Results and performance are reported.

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1. Introduction

The High Luminosity (HL) upgrade of the LHC sets stringent requirements for the CMS silicon tracker, such as higher granularity, new power distribution and trigger capabilities. In order to maintain high efficiencies and keep event rates under control for the first level of triggering, the tracker must include the capability to supply the trigger processors with track data, in the form of high transverse momentum (p_T) track primitives known as stubs. One way of identifying stubs is the stacked module approach, by which high-p_T tracks are isolated from low-p_T background by looking at the coincidence between hits on two closely separated sensors [1, 2]. Strips on both sensors are connected to alternate channels of a readout ASIC having the logic necessary for finding and reporting hit coincidences.

The CBC3 is the latest version of the CMS Binary Chip for readout of the outer radial region of the upgraded CMS Tracker at HL-LHC. It further refines the stub identification logic, first demonstrated by the CBC2 [2], and adds many new features, such as stub bend calculation, fast data output, and e-fuses for trimming and chip identification.

2. ASIC Architecture

Designed in 130nm CMOS with a bump-bondable layout, the CBC3 is a 254 input channel binary-readout ASIC with logic to correlate between odd and even channels that connect to two sensor layers of a stacked-sensor module called the 2S-module [3]. Despite the increase in functionality, the CBC3 is only 250µm wider than the CBC2. A simplified block diagram of the ASIC architecture is shown in Figure 1.

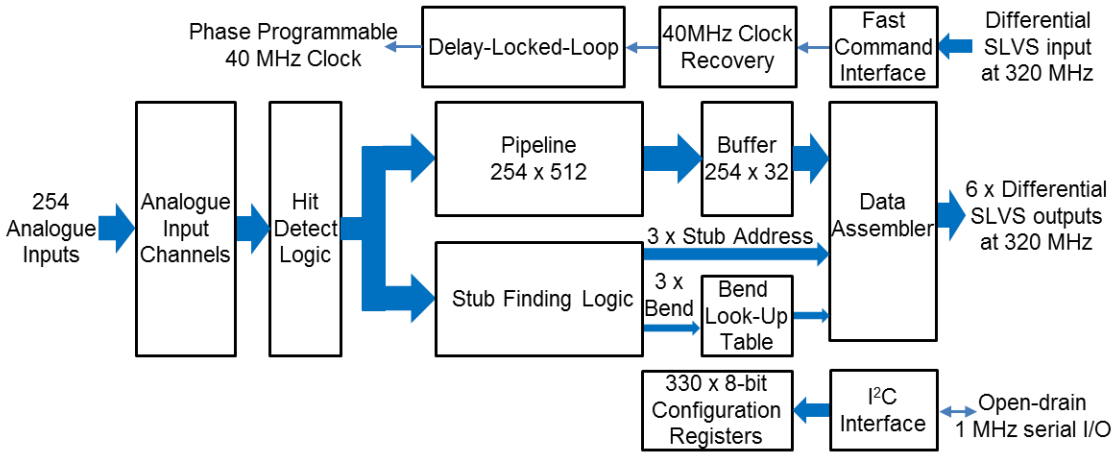

Figure 1. A simplified block diagram showing the CBC3 ASIC architecture.

2.1 Analogue Front End and Hit Detect

Each input channel comprises a preamplifier, shaper and comparator. These differ from those found on the CBC2, being intended for single polarity operation only. The preamplifier and shaper are modified to produce a shorter pulse shape, such that the pulse from a hit now recovers within 50ns, improving the deadtime performance. In the preamplifier, a regulated cascode now replaces the traditional cascode, both boosting the open-loop gain, and eliminating the need for a global cascode bias and associated trimming. The comparator has also been modified to equalise its current use between states and minimise any effect on the power supply.

The comparator outputs feed into Hit Detect logic that is optimised to efficiently capture both short duration and piled-up pulses. This logic can now suppress the effects of Highly Ionising Particles (HIPs). Channels affected by a HIP take longer than normal to recover, and consequently their comparator output can stay active for multiple bunch-crossings. The logic counts the number of bunch-crossings that the comparator output is active, and on reaching a globally set 3-bit count value, it suppresses the Hit Detect output until the comparator returns to the inactive state.

2.2 Pipeline

All Hit Detect outputs are stored in a 512-deep digital pipeline to accommodate trigger latencies of up to 12.8μs, doubling the capacity compared to the CBC2. The memory cells have been redesigned with enclosed-gate NMOS transistors to eliminate radiation induced leakage effects.

2.3 Stub Logic

The Hit Detect outputs also feed to the logic for identifying stubs. The function of this logic has been described in detail in previous publications [4]. The logic has been redesigned to provide half-strip resolution, such that even numbered clusters of hit strips are attributed a centre located between the two middle strips, avoiding the introduction of a positional bias, as in the CBC2. To match with this resolution, the correlation window size and offset is also now programmable in half-strip steps.

Stub information is further improved by the generation of a 5-bit bend code representing the offset between the matched clusters on the two sensor layers, and indicating the angle of the stub with respect to normal incidence. These are later reduced to 4-bit using a programmable look-up table.

The final stage of logic assigns an 8-bit address to the stubs, and outputs a maximum of three stub addresses along with their corresponding bend codes every bunch-crossing. Stubs are prioritised for output according to their position in the ASIC, with lower address stubs being given priority. In the event that more than three stubs are identified, a flag is output.

2.4 High Speed Interface

Transmitting stub data fast enough for the trigger processing requires a data rate greater than the 40MHz used for CBC2. A rate of 320Mb/s was chosen as a good compromise between data volume and the space available on the module for signal routing. The stub addresses and bend codes resulting from a bunch-crossing are assembled into a data packet along with a timing bit and flags, and output via five differential SLVS outputs, each operating at 320Mb/s.

For the triggered data, frames containing 254 bits of data from the pipeline, the corresponding 9-bit pipeline address, a 9-bit trigger count and two error flags are output in series at 320Mb/s via a sixth SLVS output. For synchronicity, the 2-bit data-frame header is aligned to the stub data packet timing bit. A 950ns frame period enables the CBC3 to cope with a 1MHz average trigger rate.

Fast commands are now sent via a serial command interface running at 320Mb/s, allowing one 8-bit command word every 25ns bunch-crossing. There is no encoding/decoding of the command word, and each of the four available commands, Trigger, Fast Reset, Test Pulse

Request and Orbit Reset, are identified by one of four dedicated bits. With the exception of the Orbit Reset command, these cannot be sent concurrently.

The timing for most circuits on the CBC3 is required to match the bunch-crossing rate, so a 40MHz clock is recovered on-chip from a 3-bit timing pattern sent repeatedly as part of the command word. To optimise alignment with the bunch-crossing timing, this clock is made phase adjustable in 1ns steps using a Delay-Locked Loop (DLL) circuit. The timing bit within the stub data packet is deliberately aligned with the recovered 40MHz clock.

3. Results

By varying the timing of the input test pulse for different settings of comparator threshold, the front-end pulse shape can be reconstructed. The measured pulse shape returns to baseline within 50ns as shown in Figure 2 (a). The three traces represent different settings of the shaper feedback, with the green trace being the nominal setting.

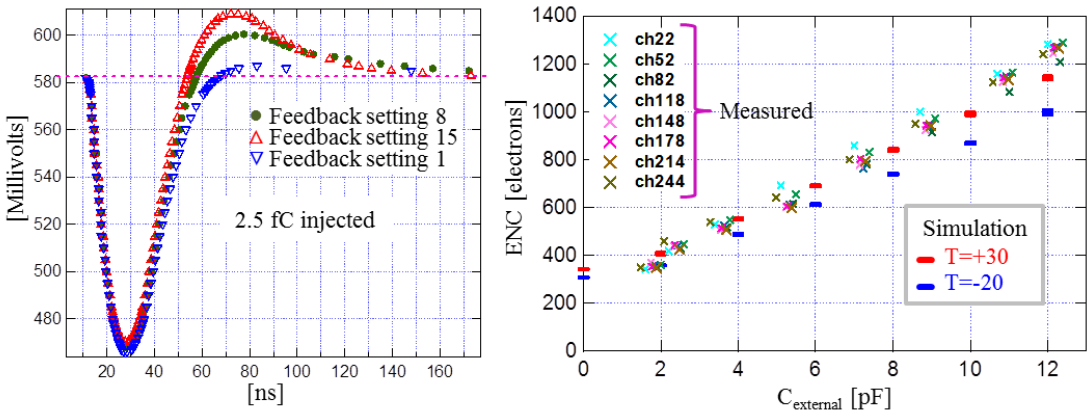

Figure 2 (a) Reconstructed front-end pulse shape, (b) Measured and simulated front-end noise vs input capacitance for eight wire-bonded channels.

The noise performance has been checked using external capacitance loads on several wire-bonded channel inputs. Figure 2 (b) shows that even with this wire-bonded configuration, the noise performance meets the specified target of 1000 electrons for a 10pF input capacitance.

Test stimuli to the chip inputs show that both the stub and triggered data can be generated in a predictable way and successfully received by the data acquisition system at 320Mb/s.

The CBC3 has been irradiated to over 400kGy with no change in analogue performance. Figure 3 shows that while there is no change in the analogue power supply current with radiation, there is an increase in the digital supply current, which decreases with continued irradiation. Tests with regions of the chip shielded confirm that this is dominated by radiation induced leakage in the standard cell logic gates of the stub finding circuits. The magnitude of this leakage current is related to temperature and rate of irradiation, and modelling of the mechanism predicts that the increase in power dissipation for the CBC3 will be less than 5mW under expected CMS operating conditions (9Gy/hour dose rate). The leakage current issues experienced with the CBC2 pipeline were no longer present, confirming that the modifications to the SRAM cells have worked.

Testing with 62MeV protons reveals that the new configuration registers are a factor of eight more resistant to Single Event Upset (SEU) than the CBC2, with an estimated SEU rate of 1.5 bit flips/chip/day at the HL-LHC.

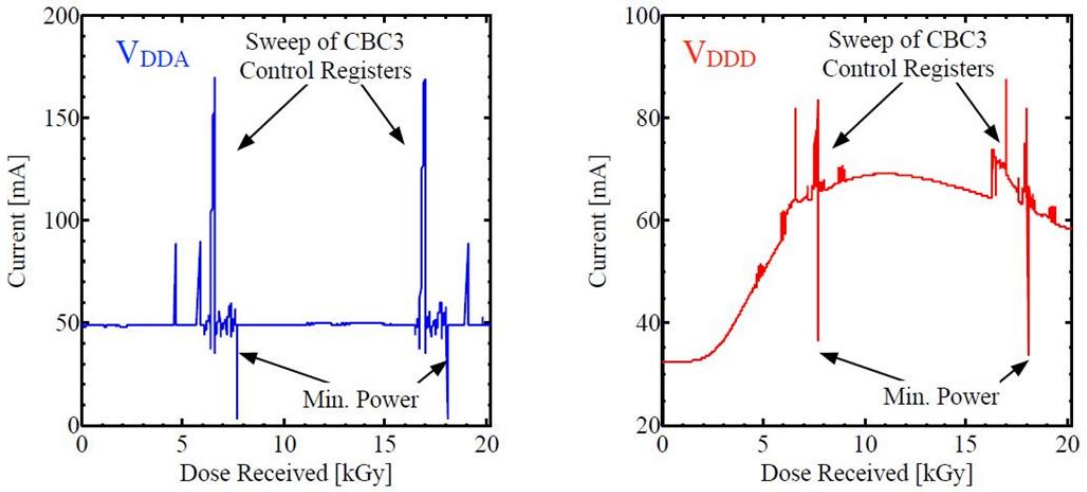

Figure 3 Analogue and digital supply current for an uncooled CBC3 irradiated at 20 kGy/hr.

4. Further Work

A number of improvements have been identified. Stubs originating outside the correlation window should be suppressed. For complete testability at wafer level the inter-chip IO must be stimulated. The timing robustness of the triggered-data output needs to be improved for a few of the 40MHz phase settings. These will be corrected in the near future with a revised version. Further improvement to the SEU robustness of the configuration registers will also be considered. Bump-bonded chips on prototype modules will be tested in coming months.

5. Conclusions

The final full size prototype of the CMS Binary Chip (CBC3) was manufactured in autumn 2016. The chip successfully integrates all of the features required for use on the 2S-module. It has been functionally tested, irradiated, and characterized using single devices wire-bonded to a test PCB, and demonstrates correct functionality to specification.

6. Acknowledgements

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