

Characterization of a 9-Decade Femtoampere ASIC Front-End for Radiation Monitoring

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An ultra-low current sensing digitizer circuit was designed for radiation monitoring for personnel and environmental safety at CERN. The Ultralow Picoammeter 2 (Utopia 2) ASIC includes some key functionalities like on-chip active leakage current compensation, charge balancing and range changing. It was designed in AMS 0.35 μm technology that was selected for its low leakage current performance. The architecture is based on the asynchronous current to frequency converter (CFC) and the front-end can digitize input currents over a wide dynamic range of 9 decades. If the measurement time is equal to 100 s, the ASIC can measure current as low as 1 femtoampere (fA). The calibration procedure and the measurements of the Utopia 2 ASIC are summarized in this article. The ASIC has been characterized for its ultra-low current performance at the Swiss Federal Institute of Metrology (METAS).

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1. Introduction

The ionizing radiation levels should be continuously monitored inside and outside CERN's premises in order to protect the public and the personnel from any unjustified exposure to radiation. Apart from particle accelerators, radiation monitoring is also important for nuclear facilities, synchrotrons, hadron therapy institutes and hospitals.

The radiation monitors at CERN consist of the ionization chambers and their readout front-end electronics. The output of the detector is a current that is proportional to the intensity of the incident radiation. According to the existing commercial detectors used at CERN by the Radiation Protection group, the front-end should be able to digitize current starting from 2 fA, since it should also measure the background radioactivity. The front-end should measure current up to a maximum value of 5 μ A. The design of an ASIC was motivated by the need to digitize input currents over a wide dynamic and temperature range and the lack of commercially available solutions.

Several readout systems for radiation detectors have been developed that demonstrate a wide dynamic range of more than 5 decades [1], [2]. However, they are limited at the picoampere range due to the input leakage currents. In order to determine the main limitations when measuring at the femtoampere level, a demonstrator ASIC named Utopia 1 was designed and characterized [3]. All the possible leakage current sources were evaluated and the dominant leakage current source in the input of the front-end proved to be the leakage current related to the ESD protection diodes [4]. According to the guidelines that the demonstrator ASIC set, a second ASIC named Utopia 2 was designed. The Utopia 2 ASIC that is depicted in figure 1(a), can measure current as low as 1 fA due to a two-channel active leakage current compensation scheme [5]. This article presents the characterization of the Utopia 2 ASIC.

2. Brief description of the Utopia 2 ASIC

The architecture of the Utopia 2 ASIC is based on the asynchronous current to frequency conversion through charge balancing. The detector current I_{det} generated from the ionization chamber is continuously integrated along with the sum of the various leakage currents on a capacitor. The output voltage V_{out1} of the integrator is compared with a voltage threshold V_{th1} using a discriminator. When the discriminator triggers, a fixed amount of charge, termed Q_{ref1} is removed from the input using a switched capacitor circuit. If the integrator's output voltage remains above the threshold, the discharging circuit injects again after recharging. A counter implemented in the FPGA counts the number of times N_1 the reference charge Q_{ref1} is subtracted from the input in a determined time window T_w , to calculate the current as shown in equation 2.1.

$$I_{in1} = \frac{N_1 Q_{ref1}}{T_w} \quad (2.1)$$

Since the dominant source of leakage current is the ESD protection diodes, the net leakage current is affected by temperature and actually doubles every 10°C of a temperature change. In order to make the low current measurements insusceptible to leakage increase due to temperature variations, a two-channel compensating principle is adopted. A second compensating channel whose input structures are matched to the measuring channel is added. This channel can subtract

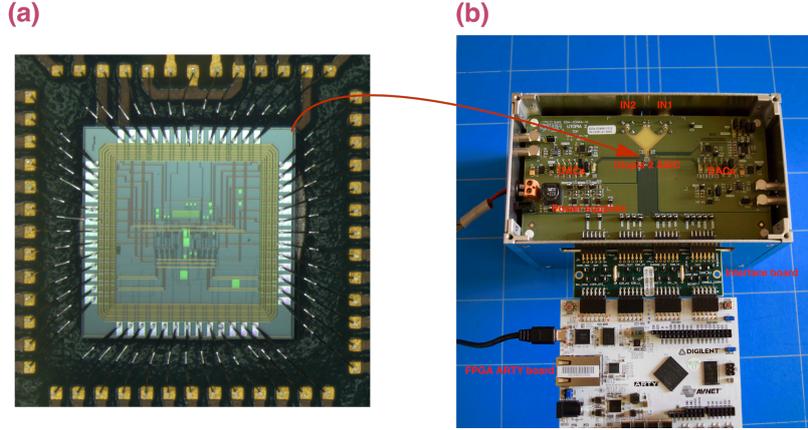


Figure 1: (a) Utopia 2 ASIC, (b) Utopia 2 PCB and DAQ board

the leakage current that it is measuring from the first channel's input and perform active leakage current compensation as shown in figure 2(a). The detector current I_{det} can be calculated using equation 2.2:

$$I_{det} = \frac{N_1 Q_{ref1} \pm \rho N_2 Q_{ref2}}{T_w} \quad (2.2)$$

where ρ is the calibrated ratio between the leakage currents of channel 1 and channel 2. The experimental setup used to characterize the Utopia 2 ASIC is based on the ARTY Evaluation board that includes an Artix-7 FPGA from Xilinx. The Utopia 2 PCB and the data acquisition (DAQ) board are shown in figure 1(b). Python routines control the operation of the DAQ system. The acquired data are then processed with Matlab.

3. Calibration procedure

The calibration procedure starts with the calibration of the reference charges Q_{ref1} and Q_{ref2} that are the most important parameters in the conversion. Channel 2 reference charge Q_{ref2} is injected into channel 1 as shown in figure 2(b). By injecting a known current from channel 2 (N_2 is known) and measuring the respective number of counts N_1 at the digital output of channel 1, the relative ratio Q_{ref1}/Q_{ref2} can be calculated by equation 3.1, where N_1 and N_2 are sufficiently big numbers. Finally to calculate the absolute value of the reference charges, a calibrated well known current in the nA range is injected into channel 1, so using the equation 2.1 the reference charge Q_{ref1} can be calculated. The Q_{ref2} is also quantified. The calibrated values will be stored for each calibrated chip and will be used for the detector current evaluation.

$$\frac{Q_{ref1}}{Q_{ref2}} = \frac{N_2}{N_1} \quad (3.1)$$

Although the two channels are designed to be matched in terms of operating conditions and layout, this is not always the case. This is why, for the active leakage current compensation the ratio ρ of the leakage currents between channel 1 and channel 2 versus temperature has to be

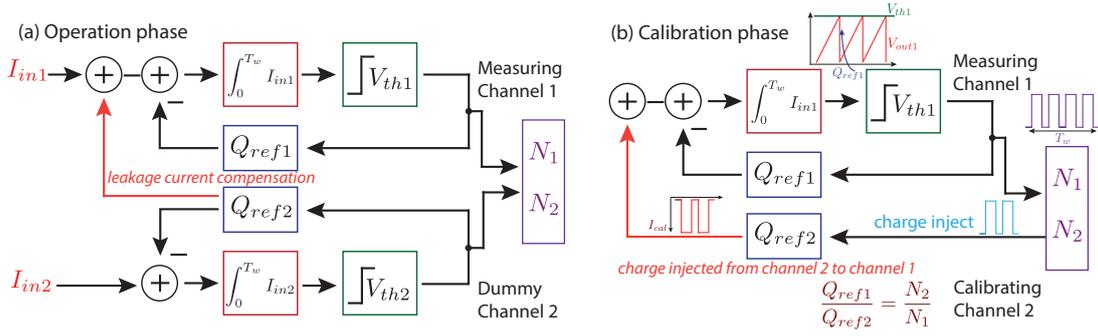


Figure 2: Simplified block diagram of Utopia 2 during (a) operation phase (b) calibration phase

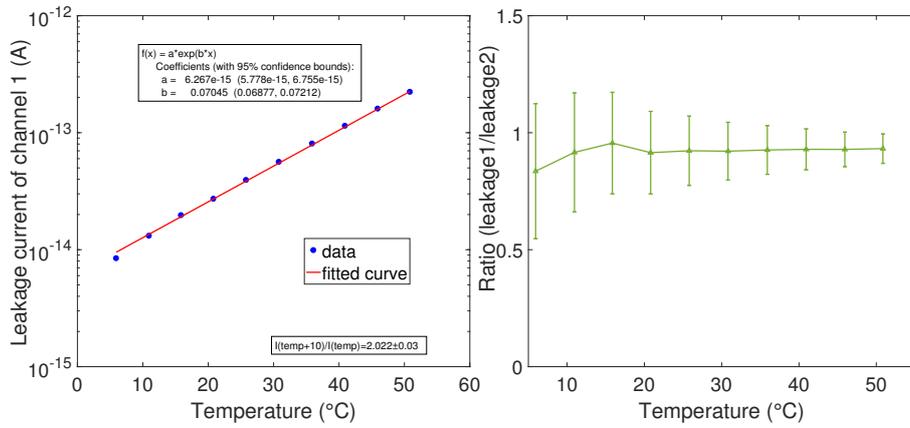


Figure 3: (a) Leakage current of channel 1 versus temperature, (b) Ratio ρ calibration versus temperature

calculated. The leakage currents of both channels are monitored inside a climatic chamber where the temperature and the humidity are controlled. Figure 3(a) shows the leakage current of channel 1 and figure 3(b) depicts the ratio ρ . The error in the ratio in the lower temperature is bigger due to lower statistics at lower leakage current for the same acquisition time. The ratio that is almost constant will determine the number of Q_{ref2} charge injections to channel 1. The ratio ρ calibration is needed for each chip to avoid any over- or under-compensation. In total, five different chips were tested.

4. Measurements

The Utopia 2 ASIC has been characterized for its low current measuring performance at the Swiss Federal Institute of Metrology (METAS), where a calibrated femtoampere current source is available. Figure 4(a) shows the measured current when the injected current ranged from -32 fA up to +32 fA. The ASIC could detect an input current as low as 1 fA. The percentage error is higher around ± 1 fA and is given as a discrepancy between the measured current value and the ideal injected current.

The ASIC was also tested with a Keithley 6430 current source that was injecting currents from 20 fA up to 6 μ A as shown in figure 4(b). The wide dynamic range behavior was verified. It can

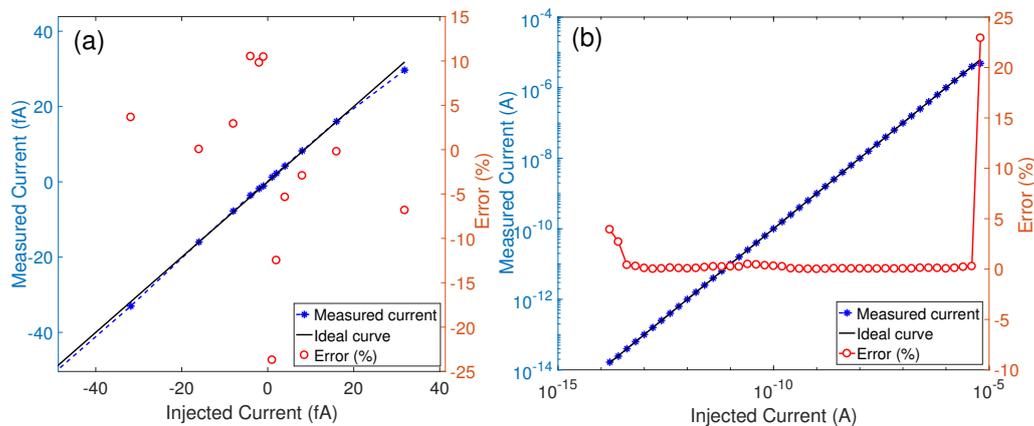


Figure 4: (a) Measurements at the METAS, (b) Measurements using a Keithley 6430 current source

be seen that the percentage error increases above $5 \mu\text{A}$ due to speed limitations.

5. Conclusions

The calibration procedure and the measurements of the Utopia 2 ASIC were presented. The front-end can measure input current that starts from 1 fA and expands over 9 decades of dynamic range. The architecture of the current to frequency converter was fully exploited and the leakage current compensation provides a leakage current free digitizer. For the sub-picoampere measurements the integrator has to integrate over more than 100 ms. The Utopia 2 ASIC fulfills the required specifications and will be used as the front-end of the new radiation monitoring system at CERN.

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