PROCEEDINGS OF SCIENCE

Characterization of SLVS driver and receiver in a 65 nm CMOS technology for High Energy Physics applications

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This work is concerned with the design and characterization of an SLVS transmitter/receiver pair, to be used for I/O links in High Energy Physics applications. Core transistors with a power supply of 1.2 V have been considered in the design in order to mitigate the TID effects, due to the harsh radiation environment foreseen. The circuits have been implemented in a 65 nm CMOS technology. The prototype chip was designed and fabricated in the framework of the RD53 project and was completely characterized in the first quarter of 2016. The chip has been also irradiated with X-rays in order to evaluate the effect of the ionizing radiation on the signal integrity

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1. Introduction

This activity has been carried out in the framework of the CERN RD53 collaboration, whose aim is the design of the next generation of hybrid pixel readout chips for the ATLAS and CMS Phase 2 pixel upgrades using a commercial 65 nm CMOS technology. The design of the readout ASIC will face several challenges: particle fluxes, radiation dose and data bandwidth become important when moving closer to the interaction point and the pixel detectors have to work in very harsh conditions. In this context, a high data-rate differential I/O link has been designed and characterized to accommodate the RD53 requirements to send data off-chip [1]. Such differential I/O link is a well-know technique used for the chip-to-chip communication at high data rates and with a low power consumption. A transmitter/receiver pair for a possible integration in the RD53A ASICs, complying with SLVS protocol, was designed and completely characterized, in the first quarter of 2016. The 65 nm proposed link will be used in a harsh radiation environment, so the design is based on thin gate oxide transistors, using a supply voltage of 1.2 V. The driver and receiver can be operated at a speed up to 1.2 Gbit/s. The SLVS standard describes a differential current-steering protocol with a voltage swing of $\pm$200 mV on a 100 Ω termination resistance and a common mode of 200 mV [2].

2. Description of the differential I/O link

The driver architecture is based on a Bridged-Switch Current Source (BSCS) scheme, as shown in figure 1[3]. The 2 mA bias current is switched through a 100 Ω termination resistance, according to the input data stream. The output current of the transmitter can be trimmed, by means of three configuration bits (`B<0>`, `B<1>` and `B<2>`), in a range from 500 μA to 2.5 mA or eventually can be fixed by means an external current source (`I_BIAS_EXT`). This feature has been implemented only for test purpose. In order to achieve insensitivity to PVT variations, a simple low power common-mode feedback has also been included. The common mode voltage is sensed by two resistors (R_0 and R_1), which are connected to the output node and compared with a reference voltage, which is generated by a resistor voltage divider. The Common Mode Feedback (CMFB) amplifier is based on a symmetrical OTA architecture. The phase margin in the nominal corner is

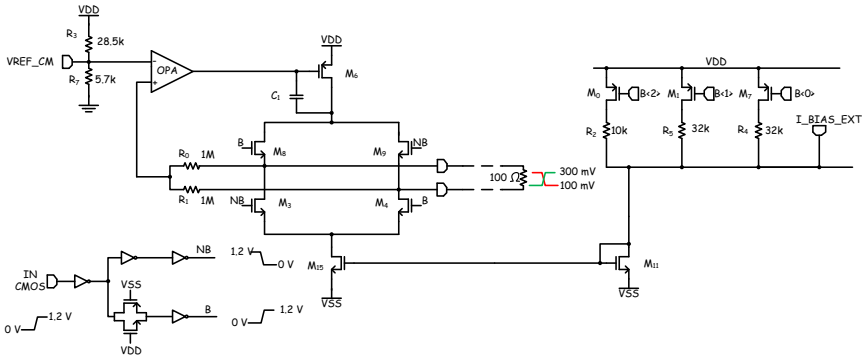


Figure 1: schematic of the transmitter.

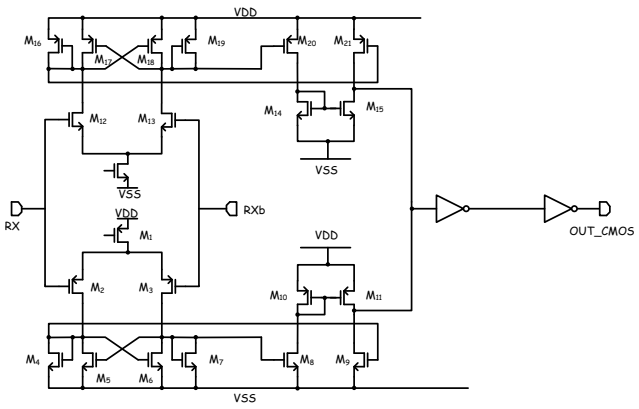


Figure 2: schematic of the receiver.

close to 80°. The receiver is a rail-to-rail stage, in order to detect differential signals with a common mode from 100 mV to 1 V. It is based on three stages, as shown in figure 2: the first one is a fully differential amplifier with a cross-coupled load and with a bandwidth close to 1.2 GHz; the second stage is a differential-to-single ended amplifier with a full swing CMOS voltage and the last one is a chain of two inverters. There is also a possibility to enable/disable the internal termination resistor with one control bit. The output of the receiver is connected to a Current-Mode-Logic (CML) buffer designed by the Microelectronics group at CERN, which converts the signal from single ended to differential. This block has been used to enable the measurement of the receiver output at high frequency.

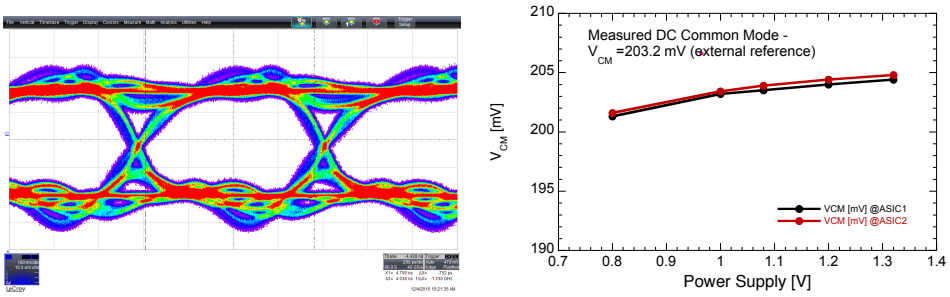
3. Characterization results

The test system consists of a PCB, which hosts two ASICs that are directly bonded on the PCB. One of the two ASICs, called ASIC1, has the output of the driver connected to the input of the receiver of the second ASIC, called ASIC2. A differential microstrip 5 cm long is used to connect the driver and the receiver. A signal generator stimulates the input of the driver with a single ended CMOS signal at 1.2 Gbit/s, while it can be used in differential mode when it is connected to the receiver input. At the same time, using a differential active probe, the eye diagram at the output of the transmitter can be measured by an oscilloscope.

3.1 Transmitter

The SLVS transmitter has been stimulated with a 1.2V CMOS PRBS signal. A differential active probe has been inserted at the end of the microstrip. Figure 3a shows the eye diagram measured at 1.2 Gbit/s. The amplitude of the eye is 377.7 mV $\pm$ 3.9 mV, the eye height is 365.1 mV. Such value implies a Signal-to-Noise ratio equal to 72, guaranteeing a sufficiently low bit error rate. The eye width, which can be related to the opening, is 752 ps. The ratio between the eye opening and the bit period is close to 0.9. The rms jitter measured from the time interval error (TIE)[1] is

[1]The TIE is a set of random time interval each one corresponding to the time difference between a real clock or PRBS and a reference ideal signal.



(a) (b)

Figure 3: (a) eye diagram at 1.2 Gbit/s of the transmitter signal (200 ps/div, 100 mV/div), (b) measured output common mode voltage (V_{CM}) as a function of the power supply (V_{DD}).

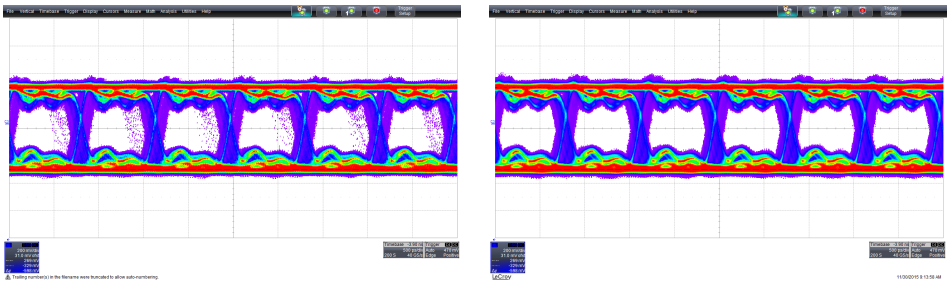
9.8 ps. The ratio between the jitter and the bit period is less than 2%. Figure 3b shows the output common mode voltage, measured in the middle of the termination resistances (the 100Ω termination resistance is composed by the series of two 50Ω resistance), as a function of the power supply variation. The purpose of this measure is to verify the robustness of the common mode feedback as a function of the voltage supply variation. Since the input common mode voltage within the driver is obtained by means of a voltage divider, an external bias (V_{CM}) has been applied to the voltage divider when the voltage supply has been changed. The output common mode voltage of the driver is kept constant by the CMFB amplifier and the voltage variation is lower than 5 mV when V_{DD} changes from 0.88 V to 1.32 V.

3.2 Receiver

The SLVS receiver has been stimulated with a differential voltage PRBS signal at 1.2 Gbit/s. The 200 mV common mode complies with the JEDEC specifications, while the differential input goes from 100 mV to 200 mV. Measurements have been performed at the output of the CML driver. The minimum detectable differential signal is 150 mV, as shown in figure 4a. Figure 4b shows the eye diagram in nominal conditions, when 1.2 Gbit/s signal with a differential mode of 200 mV is applied at the input. In this case the eye is open.

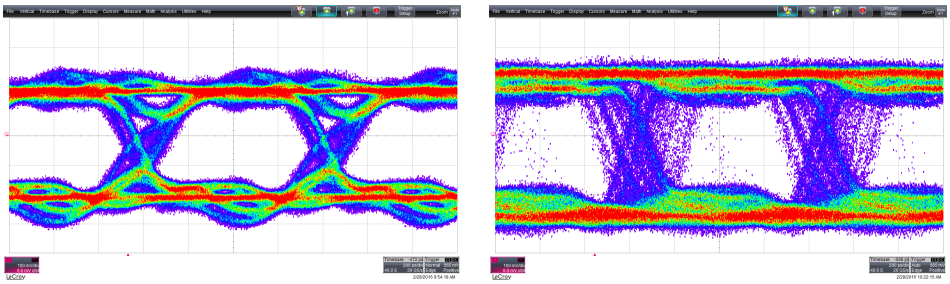
4. Irradiation results

The prototype chip was irradiated with X-rays at the CERN facility up to a total ionizing dose (TID) of 550 Mrad(SiO_2) with a dose rate of 9 Mrad/h. The building blocks are required to withstand a total dose of 500 Mrad(SiO_2)[4]. The eye diagram of the irradiated transmitter is shown in figure 5a. Before irradiation, the eye is completely open and the crossing point is located in the middle of the eye. Instead, a degradation of the rise time and fall time is shown after irradiation (but the eye is still open). There is also a degradation of the crossing point. The jitter increases from 9 ps to 25 ps, while the degradation of the amplitude is close to 18.7 mV. Indeed, the amplitude is reduced from 377.7 mV to 359 mV. The transmitter still works at the maximum frequency even after irradiation. Figure 5b shows the measurement taken at the receiver after irradiation. The eye diagram of the receiver is partially degraded. This can lead an increase of the bit error rate.



(a) (b)

Figure 4: (a) eye diagram at 1.2 Gbit/s of the receiver with a differential input of $V_{ID} = 150$ mV (worst case condition), (b) eye diagram at with a differential input of $V_{ID} = 200$ mV (nominal condition), (500 ps/div, 200 mV/div).



(a) (b)

Figure 5: Post irradiation results of the transmitter (a) and of the receiver (b) (200 ps/div, 100 mV/div).

5. Conclusions

A differential I/O link for the RD53 collaboration has been designed, fabricated and characterized in a 65 nm CMOS technology. In order to prove its capability to operate in harsh radiation environment, they were irradiated with X-rays up to 550 Mrad(SiO_2) TID. The driver and receiver still work with some degradation of the performance after irradiation. These building blocks have been integrated in the RD53A chip.

References

[1] N. Demaria, M. Barbero, D. Fougeron, F. Gensolen, S. Godiot, M. Menouni et al., *Recent progress of RD53 Collaboration towards next generation Pixel Read-Out Chip for HL-LHC*, *Journal of Instrumentation* **11** (2016) C12058.

[2] S. Bonacini, K. Kloukinas and P. Moreira, *e-link: A radiation-hard low power electrical link for chip-to-chip communication*, in *Topical Workshop on Electronics for Particle Physics TWEPP-09*, CERN-2009-06, 2009.

[3] A. Boni, A. Pierazzi and D. Vecchi, *LVDS I/O Interface for Gb/s-per-Pin Operation in* $0.35-\mu m$ *CMOS*, *IEEE Journal of Solid-State Circuits* **36** (Apr, 2001) 706–711.

[4] RD53 Collaboration, *RD53A Integrated Circuit Specifications*, *CERN-RD53-PUB-15-001* .