PROCEEDINGS OF SCIENCE

A Digital Processing Unit of a Highly Integrated Receiver Chip for PMTs in JUNO

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The Jiangmen Underground Neutrino Observatory (JUNO) is a multi-purpose underground experiment based on a 20,000 ton liquid scintillator with the one main objective to determine the neutrino mass hierarchy. The signal detection is performed by photomultipliers with directly attached readout electronics. The central component for the digitization process is a receiver chip with a low power and large dynamic range analog to digital conversion unit. The concept and design of the included data processing unit and regulation circuit are presented.

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1. Introduction

The Jiangmen Underground Neutrino Observatory (JUNO) is an upcoming neutrino detection experiment located in China that aims to determine the neutrino mass hierarchy by detecting reactor antineutrinos from two nearby nuclear power plants [1]. The central detector, a liquid scintillator of 35.4 meters in diameter is situated with 700 meters rock overburden. It is surrounded by 18,000 20-inch photomultipliers (PMTs) submerged in water, that are designed to detect the emitted light with high timing and energy resolutions. In order to preserve signal quality and reduce the number of cables in the detector, the receiver chain is integrated into the PMT housing.

A highly integrated analog to digital conversion unit (ADU) is developed in 65 nm CMOS technology with three high performance 8-bit ADCs that have a programmable gain and run in parallel in order to cover a large linear voltage input range of more than 80 dB. After digitizing and signal processing, the signal is sent through a 100 meter Ethernet cable.

Besides the control of the configuration, data processing is a major task in the receiver chip to reduce subsequent processing efforts. The concept of the main data processing unit and the baseline regulator of the ADU chip are discussed in this paper. The presented baseline regulator concept has been implemented in the second prototype and the simulation results are presented.

2. Main Data Processor Concept

Neutrinos produce photons by interacting with the scintillator. These photons generated inside the detector hit the front of the photomultiplier tube (PMT) and are converted to a current signal. This current signal is fed to the analog to digital unit (ADU) which is directly attached to the PMT.

The current is converted into a voltage signal and amplified further by the front-end transimpedance amplifier of the chip. The analog voltage signal is then sampled and encoded in 8-bit binary data by the analog to digital converter (ADC) and the following encoder.

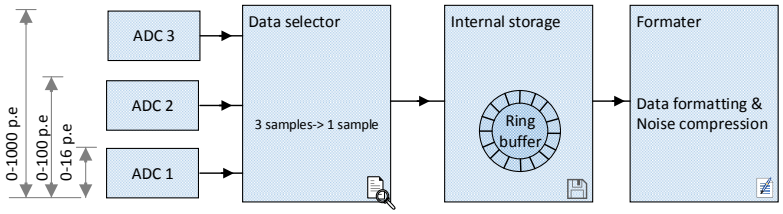

Figure 1: Schematic of the main data processor for the three ADCs covering different signal charge ranges

Based on the requirement specifications of JUNO [1], an upper limit is set to a signal amplitude equivalent of 1000 photoelectrons (p.e.) per channel. Until 100 p.e., a linear charge resolution in the range of 0.1-1 p.e. is required and above 100 p.e., it is expected to be 1%. The required high dynamic range is achieved by using three ADCs with different programmable gains in parallel as indicated in Figure 1. While the combination of parallel ADCs provides a large dynamic range, it is sufficient to only send data from one of the three ADCs for signal reconstruction.

An on-chip data processing unit is included to judiciously select data from one of the three ADCs and to generate meta data to identify the gain of the ADC during data reconstruction. Addi-

tionally other system events like counter overflows are encoded in the meta data field. In the main data processing unit, binary data from the analog to digital encoder is processed in three stages.

By default, data from "ADC 1" is transmitted. At every sampling instance, data samples are compared across three programmable threshold levels: noise level, high gain level and medium gain level in the data selector. If the signal amplitude crosses high gain threshold or medium gain threshold, data is selected from "ADC 2" or "ADC 3" respectively. When the signal amplitude falls below the thresholds, the data selector selects the data from the unsaturated ADC with best resolution.

In the second stage of the processor, data is prepared for reconstruction. The source of the sample as well as timing and trigger information is appended to the data and stored in the internal buffer.

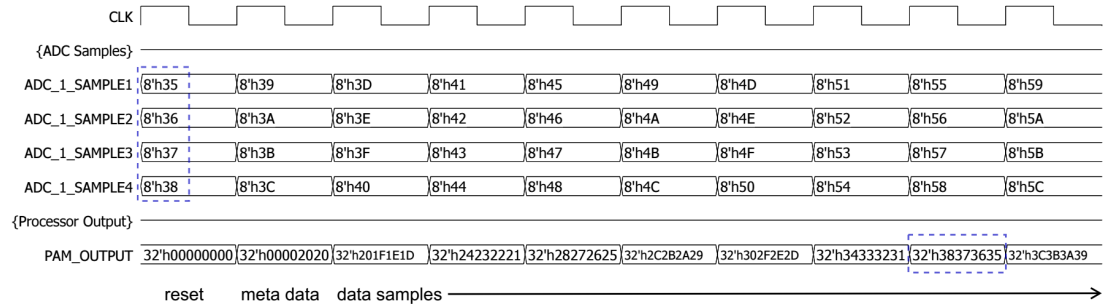

Figure 2: An exemplary data transmission with the clock signal, data samples from "ADC 1" and the output of the processor are shown. The transmission begins with a reset signal followed by meta data and data samples. Input data samples and their corresponding position in the output stream is highlighted in blue.

In the third stage, the data stream is formatted for the output. On the occurrence of trigger events or threshold crossings, meta data is sent ahead of the corresponding data. In the exemplary waveform shown in the Figure 2 it can be observed that in addition to the processing time, the transmission of reset word and meta data adds an overhead before the sampled data appears on the output. An internal buffer is added to buffer data during the overhead time and is designed to cover even the most extreme scenarios of increased data rates that occur during galactic supernova events.

Each meta data word transmission increases the latency, filling the internal buffer. During the absence of a light signal, data samples below a noise threshold are identified by the processor and compressed by a factor of two in the third stage of processing. This counteracts the overhead generated by the meta data and reduces the occupancy of the buffer.

3. Results of Laboratory Measurements

A chip prototype was designed and fabricated. The data processor was measured by the internal waveform generator that allows programming waveforms to various entry points in the processing chain. Different possible scenarios were fed to the processor to verify the functionality. The

measured raw data is then imported into MATLAB to interpret and visualize it as shown in Figure 3. The silicon verification of the main data processor demonstrated the desired data selection scheme and noise compression. A data reduction from 3 Gb/s to 1 Gb/s is achieved by a conditional data selection during signal measurement mode and a further data reduction to 0.5 Gb/s is achieved by compressing data during the absence of the light signal [1]. The main data processing unit from the first ADU prototype was measured and verified for functionality in the lab.

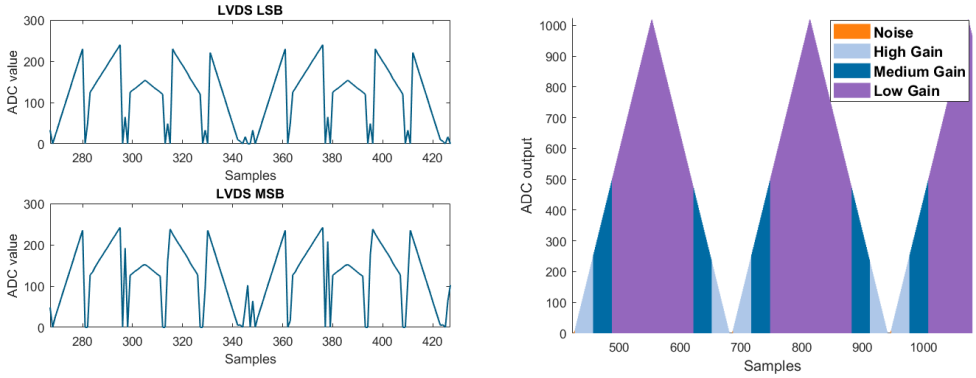

Figure 3: The left plot shows the raw data output of the processor from the first prototype. The right plot shows visualization of the corresponding data in MATLAB with reconstructed gain settings

4. Improved Baseline Regulator Concept

The effective charge of the particle is measured by integrating the current signal over time from the baseline. Biasing fluctuations and intersymbol interference may introduce an offset in this baseline. By correcting the offsets online, digitization error, intersymbol interference and reduction of ADC range due to the offset is minimized. This is realized by a real-time digital sigma-delta-based ADC baseline regulator that is included in the chip.

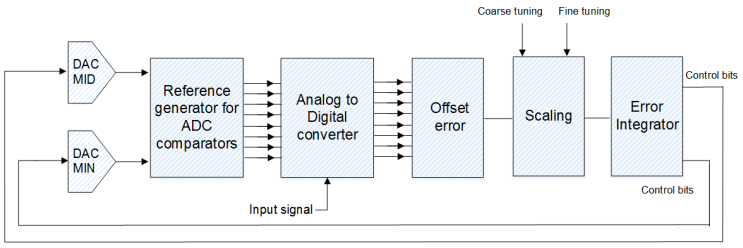

Figure 4: Schematic of the baseline regulator correcting baseline drifts online

An error signal is generated in a control loop by calculating the differences between the actual and the desired baseline. A control signal proportional to the error signal is then generated which in regular control loops would be used to adjust the input signal. However, this regulator design show in the Figure 4 adjusts the reference voltages of the ADC proportional to the offset.

Compared to the first version of the regulator that is described in [2], where the error signal generation was halted after matching the desired baseline value, the baseline is continuously reg-

ulated based on the sigma-delta modulation principle in the improved version. The average of the baseline then represents the desired baseline as shown in Figure 5.

The error signal is scaled before the error integrator part of the control loop. The settling time of the control loop is proportional to the scaling factor used. A faster settling time is achieved by larger scaling factor (coarse tuning) and better tuning is achieved by using a smaller scaling factor (fine tuning). The regulator automatically switches between coarse and fine tuning based on the magnitude of the error signal. Simulation results presented in the Figure 5 show that the correction of baseline is achieved by the the described baseline regulator.

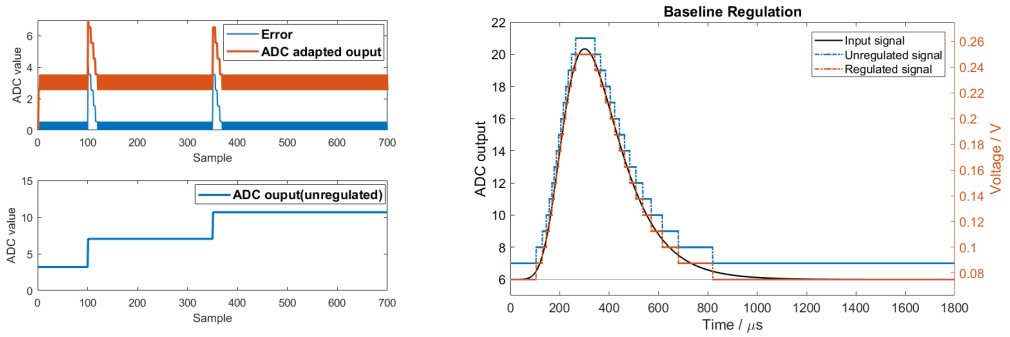

Figure 5: The left plot shows the adaptation of the ADC output in response to the error signal. The average of the regulated ADC reaches the desired baseline of 3 even after introducing artificial errors, indicated as steps in the lower plot. The right plot shows a pulse with an offset of a previous pulse (blue). The offset is corrected for the 2nd pulse by the regulator (orange).

5. Conclusions

This work presents the architecture of a custom data processor, selecting data from three parallel ADCs. A customized data selection performed by the processor aids to efficiently utilize the whole dynamic range while reducing the output data rate. The verification of the produced first prototype shows a processor complying to the required functionality. In addition to the processor, the architecture of an improved on-chip baseline regulator has been presented. With the proposed realtime baseline correction, the dynamic range of the ADC is not reduced by baseline drifts and can be solely used for signal digitization and with a higher precision than the regulator in the first prototype.

6. Acknowledgments

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References

[1] Zelimir Djurcic et al. JUNO Conceptual Design Report. 2015.

[2] P Muralidharan et al. An Automatic Baseline Regulation in a Highly Integrated Receiver Chip for JUNO. *Journal of Physics: Conference Series*, 888(1):012051, 2017.