PROCEEDINGS OF SCIENCE

Design and Test of a 65nm CMOS Front-End with Zero Dead Time for Next Generation Pixel Detectors

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This work is concerned with the experimental characterization of a synchronous analog processor with zero dead time developed in a 65 nm CMOS technology, conceived for pixel detectors at the HL-LHC experiment upgrades. It includes a low noise, fast charge sensitive amplifier with detector leakage compensation circuit, and a compact, single ended comparator able to correctly process hits belonging to two consecutive bunch crossing periods. A 2-bit Flash ADC is exploited for digital conversion immediately after the preamplifier. A description of the circuits integrated in the front-end processor and the initial characterization results are provided.[†]

Topical Workshop on Electronics for Particle Physics
11 - 14 September 2017
Santa Cruz, California

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[†]This manuscript has been co-authored by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics.

PoS(TWEPP-17)021

1. Introduction

Next generation pixel chips at the HL-LHC will operate with extremely high particle rates and radiation levels. In the so-called Phase II upgrade, ATLAS and CMS will need a completely new tracker detector, complying with very demanding operating conditions and a high delivered luminosity (up to 5×10^{34} cm^{-2}s^{-1} in the next decade). Very low noise performance of the analog front-end, along with stable low threshold operation, will be key points for highly efficient readout chips. The 65 nm CMOS technology has been identified by the ASIC designer community as the candidate process for the development of future readout chips at the HL-LHC [1]. This technology retains the good degree of tolerance to ionizing radiation that is typical of CMOS nodes in the 100 nm regime [2] and enables the integration of dense in-pixel analog and digital functions.
A synchronous analog front-end with zero dead time, called IFCP65, has been designed in a 65 nm CMOS technology in the framework of the CERN RD53 collaboration [3]. A prototype chip, including a 16×16 pixel matrix, has been submitted and tested. A description of the main blocks of the analog front-end processor and results from the experimental characterization are provided in the following sections.

2. Analog front-end

The analog processor, whose schematic diagram is shown in Fig. 1, includes a charge sensitive amplifier (CSA) based on a regulated cascode gain stage, and features a leakage current compensation circuit able to deal with the large radiation-induced increase in detector leakage. A source follower stage is exploited for properly driving the CSA load. The signal at the CSA output is fed to a fast threshold discriminator, operated with a 40 MHz clock, which provides hit/no-hit information at the channel output. The particular implementation of the comparator is ideally insensitive to device threshold voltage mismatch, hence no threshold-tuning DAC has been included in the pixel cell. A 2-bit flash ADC is exploited for digital conversion in this shaper-less analog front-end. The ADC design is based on three comparators with the same architecture of the hit comparator, resulting in a full analog-to-digital conversion lasting 12.5 ns, and making this device extremely attractive for those applications where the dead time has to be minimized. In the submitted prototype the ADC can be turned off, thus enabling a pure binary operation of the readout channel.

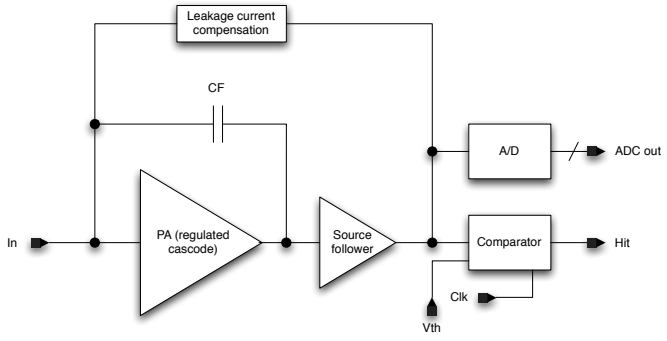

Figure 1: Block diagram of the IFCP65 readout chain.

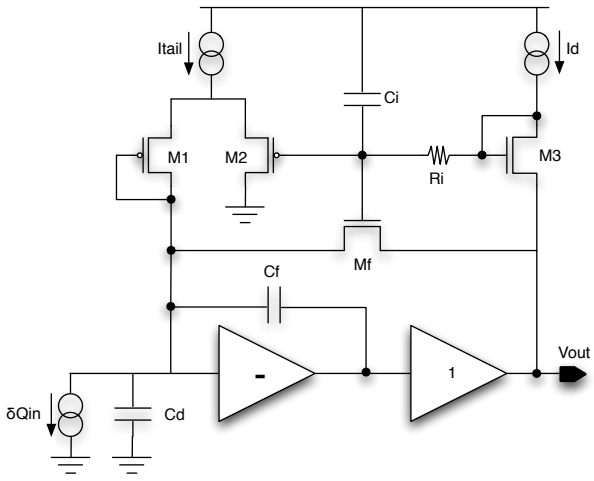

Figure 2: Schematic of the IFCP65 charge sensitive amplifier, featuring a leakage current compensation network able to deal with a detector leakage up to 14 nA.

3. Characterization results

A thorough characterization of the front-end processor has been carried out on a prototype chip integrating a 16×16 pixel matrix. Measurement results on the CSA and on the threshold discriminator are provided in the following.

3.1 Charge sensitive amplifier

The schematic diagram of the charge sensitive amplifier is shown in Fig. 2, with particular emphasis on its feedback network. The active feedback transistor, M_f, acts as a $1/g_m$ resistor for small signals, g_m being the transconductance of M_f itself, whereas it behaves as a constant current source for large signals. The preamplifier input is shunted with a programmable capacitance, C_d, emulating the presence of the detector capacitance. A complete description of the CSA is given in [4], where the presented simulation results show that the leakage compensation network is able to cope with the expected increase in detector leakage after irradiation. The nominal current con-

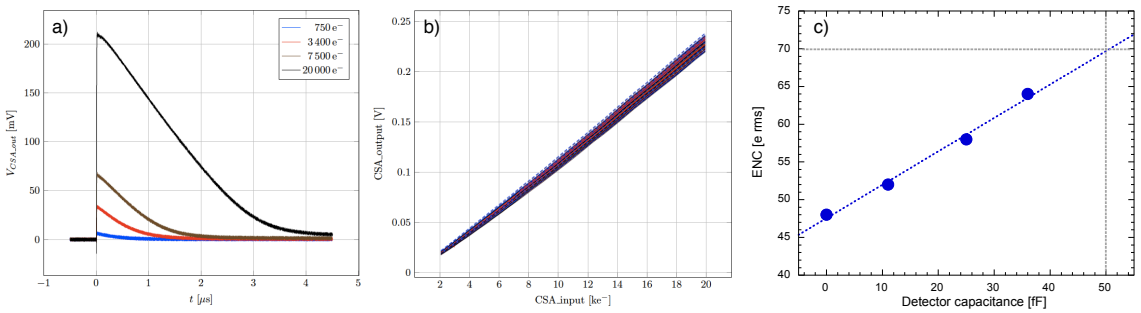

Figure 3: a) CSA response to different input charges, ranging from 750 to 20000 electrons. b) CSA peak amplitude as a function of the injected charge, for all the pixels in the 16×16 matrix. c) Equivalent noise charge as a function of detector capacitance C_d.

sumption of the charge sensitive amplifier is 4 μA, with a power supply voltage of 1.2 V.
Fig. 3a) shows the preamplifier output for different values of the input charge, injected with an external pulser via an in-pixel 11 fF injection capacitance. The rise time, evaluated for a signal of 750 electrons, is close to 5 ns with a 25 fF detector capacitor shunting the CSA input. The time to return to the baseline increases, as expected, with increasing input charge, since the feedback capacitor C_F is discharged by a constant current for large signals. The recovery time, close to 4 μs for the 20000 electrons input charge, can be adjusted by properly setting the value of the I_d current flowing in M3 transistor. It has to be noticed that this quite long recovery time does not prevent the comparator from discriminating successive hits thanks to the AC coupling between the two blocks. Fig. 3b) shows the preamplifier peak amplitude as a function of the injected charge for all the pixels in the 16×16 matrix. For each pixel, the charge sensitivity, defined as the slope of the fitting straight line of the transcharacteristic curve, has been extracted leading to an average value equal to 11.0 mV/ke$^-$, with a standard deviation of 0.21 mV/ke$^-$.
The equivalent noise charge (ENC) has been evaluated by dividing the r.m.s. preamplifier output voltage noise by the extracted charge sensitivity. Fig. 3c) shows the ENC measured for different values of C_d. By linearly fitting the noise data it is possible to extrapolate a value of 70 electrons r.m.s. for a target detector capacitance of 50 fF. This makes the circuit compliant with the specifications set by the RD53 collaboration for the design of readout chips for the ATLAS and CMS innermost tracker upgrades [5], which requires a noise occupancy not exceeding 10^{-6} at a 600 electrons minimum stable threshold.

3.2 Threshold discriminator

The charge sensitive amplifier is AC coupled to the hit comparator, which can be used to provide a binary readout. The comparator, whose schematic diagram is shown in Fig. 4a), is operated in two different phases, controlled by a clock signal driving three switches, and features a current consumption close to 1 μA. In the first reset phase, lasting 12.5 ns with a 40 MHz clock, the dis-

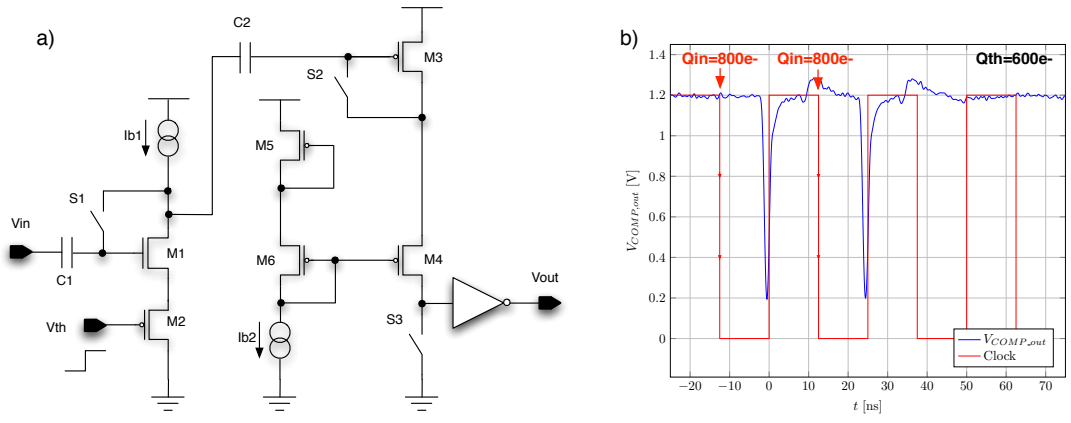

Figure 4: a) The IFCP65 comparator schematic diagram. This circuit is used both for the hit comparator and for the set of comparators included in the flash ADC. b) Comparator output for 800 electrons signals in two adjacent bunch crossing periods.

criminator gets reset and properly biased. During this phase, S_1, S_2 and S_3 are closed. During the second phase, an active comparison takes place between the signal from the CSA and the threshold voltage step, V_{th}, generated locally in each pixel of the matrix. All the switches are open during this phase. The result of the comparison is a negative going signal at the drain of M1 for preamplifier output signals larger than the threshold step amplitude. Such a signal is further amplified by M3 transistor. A detailed discussion on the discriminator operations is given in [4].
An unique advantage of the IFCP65 front-end is its capability to correctly process signals belonging to adjacent bunch crossings. This is demonstrated in Fig. 4b), which shows the measured comparator output (blue curve) in response to an input charge of 800 electrons, injected synchronously with the first falling edge of the clock signal (red curve), followed by a signal of the same amplitude in the following bunch crossing. A 600 electrons threshold was set for the measurement.
Threshold dispersion properties of the readout channels have been evaluated from the comparator efficiency curves. A threshold dispersion of 300 electrons r.m.s., significantly larger than expected, has been measured. The smaller value revealed from circuit simulations was actually obtained by optimistically setting a positive mismatch correlation coefficient between M3-M5 and M4-M6 transistor pairs in the second stage of the comparator.

4. Conclusions

A prototype chip called IFCP65 was submitted in a 65 nm CMOS technology in the framework of the RD53 Collaboration. A comprehensive characterization of a 16×16 matrix has been carried out showing very promising results, in particular in terms of noise performance, for the charge sensitive amplifier integrated in the readout channel. An equivalent noise charge close to 65 electrons r.m.s. has been measured for a detector capacitance of 36 fF, well below the limit set by the RD53 consortium for the design of the readout chips for the ATLAS and CMS innermost tracker upgrades. A fast comparator, AC coupled to the preamplifier, has been shown to be able to discriminate signals in adjacent bunch crossing periods. A partial re-design will be required to address a minor design issue in the second stage of the comparator causing excessive threshold dispersion.

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