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ASICs and Readout System for a multi Mpixel single photon UV imaging detector capable of space applications

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Large aperture MCP based UV single photon imaging detectors are commonly used in space applications and are under consideration for potential future NASA missions, such as LUVOIR, HABEX, and CETUS. For future space exploration missions, a particular interest resides in state of the art detectors with a large geometrical acceptance, spatial resolution in micro-meters, and able to operate at MHz counting rates. We are developing an imaging UV single photon detector with an aperture of 50 x 50 mm^2, and ASIC chips which enabled the construction of it's readout system. The system is composed of fast, low noise and low power 16 channel CSA amplifier ASICs, and 16 channel GSPS waveform sampling and digitizing ASICs. The detector and readout system are currently under evaluation. This paper presents the ASICs, readout system design, and first results from the detector.

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1. Introduction

The Department of Physics and Astronomy (ID Lab) at University of Hawai'i and Space Sciences Laboratory, Berkeley, collaborate on the development of a UV single photon imaging detector. The detector uses a photo-cathode to convert single photons into photo-electrons and a Micro Channel Plate (MCP) stage for charge multiplication. The incident photons position is extrapolated by measuring the charge cloud distribution for every event, over orthogonal anode strips being 25 μm wide and 625 μm apart [1].

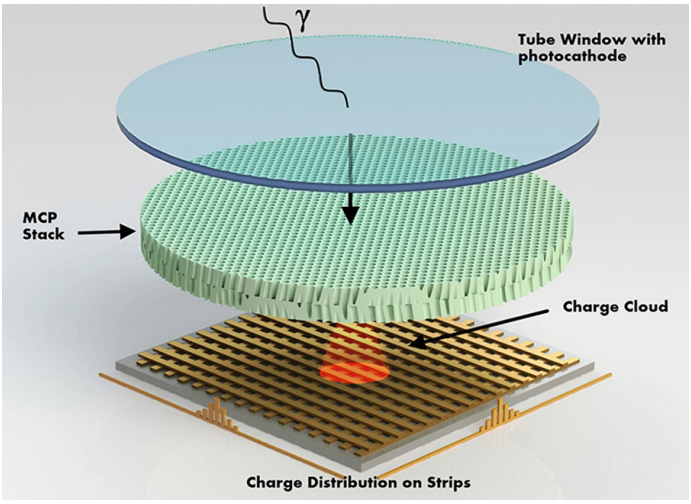

Figure 1: Schematic view of a detector comprising of an entrance window coated with a photo-cathode, MCP stack, and cross strip anodes.

Using an older laboratory readout system (Parallel Cross Strip - PXS), a spatial resolution of 17 μm FWHM was measured [2]. Our base line detector has an aperture of 50 x 50 mm^2, therefore the readout system must continuously measure 160 channels. Space grade instruments are required to operate at very low power, low noise, and enable high count rates. A readout system, which would increase the technology readiness level (TRL) from 4 to 6, would enable prototyping with real scale systems [3]. Table 1 summarizes its key parameters.

Table 1: TRL 4-6 Readout system requirements:

Channel analog input dynamic range	0 - 50 fC (AC or DC coupled)
Channel detector capacitance	5 pF
Amplifier gain	10 mV/fC (higher options desirable)
ENC	$<=$ 1000 e$^-$ at 5 pF detector capacitance
Signal sampling frequency	1 GHz
Internal memory/channel	8 μs
ADC resolution	10-bit +, S/N $>$ 50 dB
Event rate	1 M event/s
Power consumption	$<$ 50 mW / channel

We have developed a 16 channel Charge Sensitive Amplifier (CSA) ASIC in 130 nm TSMC-CMOS technology. It features an input linear range up to 50 fC of charge, baseline gain of 10 mV/fC, noise figure of 600 e-, analog output pulse rise time of 25 ns, and power consumption of 5 mW per channel [4]. Its partnering ASIC, called HalfGRAPH, is a 16 channel Giga Sample Per Second (GSPS) waveform sampling and digitizing ASIC, to a large degree similar to the TARGET ASIC[5] The sampling capacitor array, along with an analog storage array, enables the ASIC to keep about 8 μs of data per channel. In addition, HalfGRAPH has built in programmable signal over threshold triggers which group 4 consecutive channels in order to provide a temporal and a coarse event position. An external FPGA circuit is necessary to operate the system, and to access the HalfGRAPH's analog memory array, convert the stored values using the ASIC internal 12-bit (Wilkinson) slope converter, and readout the data over serial interfaces. Converting only the data region of interest enables efficient data transmission reduction, increases single photon counting event rates, and finally reduces power consumption. HalfGRAPH is designed in 250nm CMOS technology [6].

2. Readout System

Both chips are highly integrated and programmable in order to reduce the required external biasing components for operation. Using these ASICs we constructed a self trigged readout system, which is presently under evaluation coupled to the 50 x 50 mm^2 detector. The 160 channel system constitutes of 10 CSAs and 10 HalfGRAPHs. The total power consumption is 12 Watts, including the two ARTIX 7 FPGAs required for controlling the system. Figures 2,3,4 show the analog board hosting 10 CSA ASICs, the digital board with 10 HalfGRAPHs and two FPGAs, and the readout system stack attached to the detector chassis.

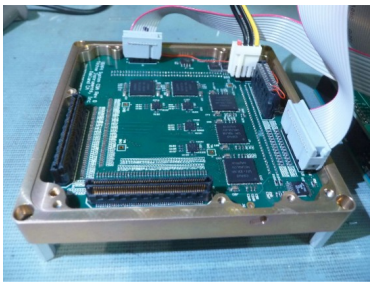

Figure 2: Analog board containing 10 CSAv3 amplifiers

Figure 3: Digital board containing 10 HalfGRAPHs and 2 Artix FPGAs

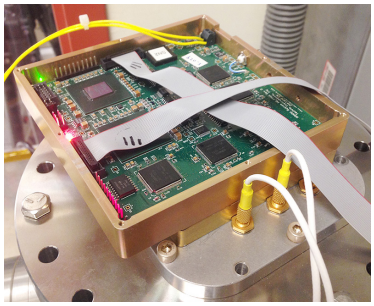

Figure 4: Electronic readout attached to the back end of the detector.

The system provides two modes of operation. The first mode provides calibration by injecting charges at the CSA inputs, providing a predictable response to verify the overall correct operation. The second is a data acquisition mode, where photons entering the detector generate triggers and the system provides the digitized data.

It is worth mentioning that this system can be scaled for larger detectors. Doubling the number of ASICs quadruples the detector's active surface. A new 100 x 100 mm^2 aperture detector with a 320 channel readout system are also under construction [7].

3. Results

The CSA amplifier ASIC [4] and HalfGRAPH were tested separately on a smaller system [6], and found to comply with the requirements except for the event rate capability, which is still under evaluation, as it partially depends on the algorithms on the FPGA. The ASIC has a linear input range of 1.5V and a digitizer providing a resolution of 10 functional bits out of 12. The overall Equivalent Noise Charge (ENC) contribution of the electronic readout system is about 1200 e^-. Given the fact that the analog pulse is substantially oversampled, averaging samples enables reduction of the noise to acceptable level. Figure 5 shows the detector's X(bottom 80 channels) and Y (top 80 channels) axes as a function of time (128 samples at 1ns/sample). The left-most image is raw data, next is the pedestal values (static offset of the digitizer), the third is the signal with the pedestal subtracted, and fourth is an event represented in a 3D plot, where color depth represents signal magnitude. Looking closely at one axis for a similar event (Fig.6) one can clearly see the charge cloud being spread over multiple (6) of channels.

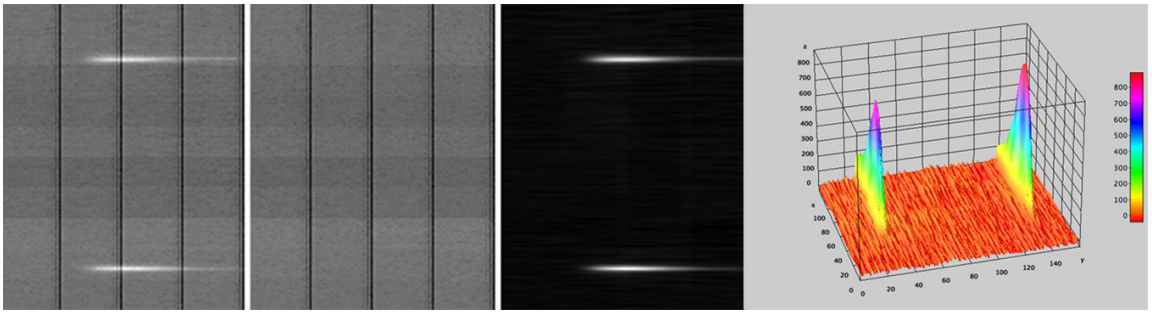

Figure 5: Response of the detector to a single photon in time domain from raw data to 3D magnitude plot as a function of time.

Both chips were recently irradiated with gamma rays following MIL-883 standard for testing electronic equipment exposed to ionizing radiation. The CSA received a dose above 200 kRads, while the HalfGraph was irradiated with 225 kRads. Both passed the test without observable functional or performance issues and could qualify for Jupiter missions with appropriate shielding. Currently, we are implementing the algorithm for the photon position extraction, with time of arrival, and cumulative charge magnitude for each event.

4. Conclusion

We designed and tested the ASICs, constructed a scalable low noise and low power readout system to instrument a large aperture single photon imaging detector, and performed radiation tests to prove its capability to operate in space like environment. The system meets the design requirements and its presently undergoing performance and functional tests. To further decrease the power consumption, reduce the system complexity and shrink the package footprint, we are designing a new ASIC called GRAPH. The GRAPH ASIC will encapsulate the 16 channel CSA design with a new waveform sampling GSPS ADC on a single die using 130nm TSMC technology.

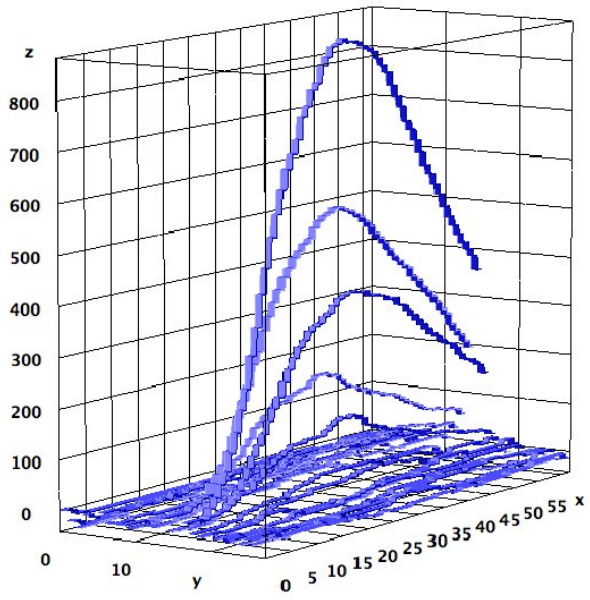

Figure 6: Response of the system to single photon, close view on excited channels, z= magnitude, y=channel, x=time [ns].

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