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Prototype chip for a control system in a serial powered pixel detector at the ATLAS Phase II upgrade

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A new inner tracking detector for the Phase-II upgrade of the ATLAS experiment is in development. A serial power scheme is foreseen for the pixel detector. This requires a new detector control system to monitor and control the pixel modules in the serial power chain. The Pixel Serial Power Protection (PSPP) chip is an ASIC for this purpose. It operates parallel to the modules and contains an ADC and bypass transistor. This paper presents test results for the prototyped PSPP chip. It includes irradiation up to 600 Mrad total ionizing dose and long-term measurements. The third version of the PSPP chip is functional and will be used for tests with serial power chains together with pixel modules.

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1. Introduction

A new Detector Control System (DCS) is in development at the University of Wuppertal for the Inner Tracker (ITk) pixel detector of the ATLAS phase II upgrade. One main change compared to the current detector is the usage of a serial power chain [1, 2]. A constant current source provides power for all modules, each having its own reference voltage. This requires AC coupled communication lines. Furthermore a single module failure could affect the whole chain. The control path of the DCS allows to monitor and to control individual modules [3]. This independent path consists of the Pixel Serial Power Protection (PSPP) chip and the DCS controller chip. The PSPP is parallel to each module and monitors the voltage and temperature of the module. With a bypass transistor it can deactivate a single module in case of failure. The DCS controller acts as a bridge between the PSPP chip and the computer in the counting room [4].

2. Prototype for the pixel serial power protection chip

The PSPP chip is an ASIC designed in a 130 nm technology to operate in a serial power chain and to monitor pixel modules [4, 5]. Figure 1 shows the block diagram of the PSPPv3. The third version includes updated elements: a radiation hard bypass transistor supporting up to 8 A, an automated bypass activation when module voltage or temperature rise above a fixed threshold and updated logic core with triple modular redundancy (TMR) to protect against the effects of single event upsets (SEUs). The communication with the controller is done with three AC coupled single ended lines. We tested successfully the communication with a serial power chain including 16 PSPP, which is the maximum of chips addressable in one bus. All chips are powered with a single supply line and the return is merged into the serial chain current.

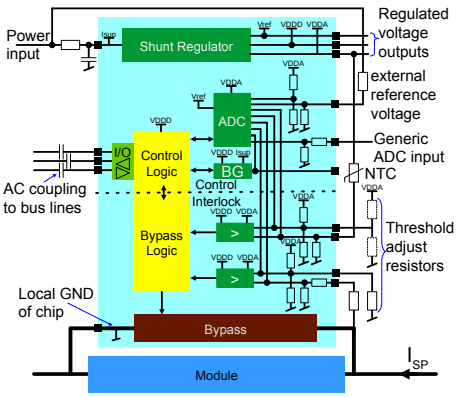

Figure 1: Block diagram of the PSPPv3 chip.

The PSPP Add-on Regulator and Comparator (PARC) includes the remaining radiation hard elements required which weren't ready for the PSPPv3. It contains a shunt regulator for the operation in the serial power chain, together with a linear regulator and a comparator circuit. Figure 2 shows that the regulator voltages are working as specified.

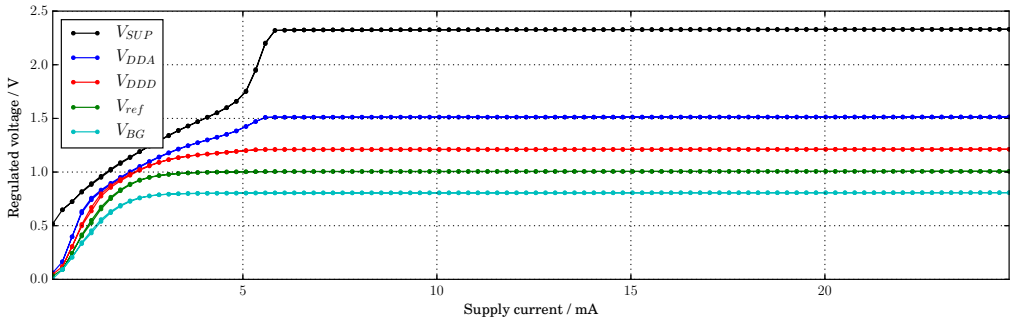

Figure 2: Measured PARC regulator voltages as function of the input current.

3. Reliability measurements with the PSPPv3 and PARC chips

The PSPP was tested to verify operation in environments similar as expected at the ITk pixel detector.

3.1 Long-term tests

A single PSPPv3 was tested in a climate chamber at different temperatures, each for 7 days of continuous operation. The bypass was activated for 23 h and deactivated for 1 h every day. A dummy module consisting of a 0.25 Ω resistor was in parallel to the PSPP under test. The serial current was kept at 3A. The communication with the chip was verified and the ADC channels were read in periodic intervals of 15 s. The test was performed at 0 °C, 30 °C and 50 °C. Figure 3 shows the measured bypass resistance. The peaks seen in the plot are times at which the bypass is switched off. At these times the resistance of the dummy module is measured. The on-resistance is very constant over the entire measurement with a variation of 0.1 mΩ, though there is a dependency on the temperature of the chip. The maximal on-resistance is around 20 mΩ which could still be improved to reduce the power dissipated at the maximum current.

3.2 Irradiation tests

The PSPPv3 and PARC chips were irradiated with a Precision X-Ray X-RAD iR160 biological irradiator at CERN up to a total ionizing dose (TID) of 600 Mrad. We decided to irradiate first at a

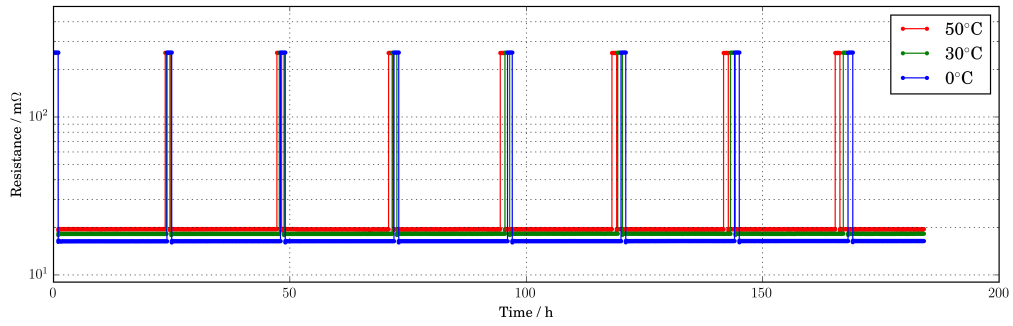

Figure 3: Bypass resistance over all long-term measurements.

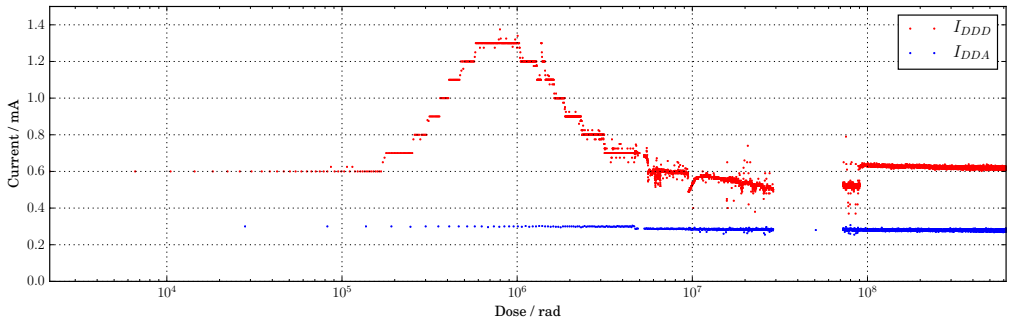

Figure 4: Analog and digital supply current of the PSPPv3 during irradiation. The gap around 30 Mrad to 70 Mrad was because of program problems. At ca 90 Mrad the interval to read the chip was increased, which led to higher digital activity and thus higher current.

low dose rate of 235 krad/h as the used CMOS process is known to have radiation induced effects within the first few Mrad. After a TID of ca 10 Mrad we increased the rate to 3.2 Mrad/h until the full dose was reached.

We observed a rise in the digital current, which is expected due to the RINCE effect [6]. No rise was observed in the analog current, which can be explained by the usage of larger size transistors in the analog parts. Figure 4 shows the analog and digital supply current for the entire irradiation.

The chip was operated as to be expected in the experiment. The internal register and all ADC channels were constantly read. The communication worked throughout the entire irradiation and the ADC was functional too. The bypass was not switched. The bypass was tested before and after irradiation. We observed an increase of 6 mΩ in the on-resistance.

The irradiation of the PARC showed a problem with the band gap. The measurement shown in Figure 5 indicates a rise of the regulated output voltages. The regulators generate their output voltage based on V_{BG}. Figure 6 shows that the ratio between the band gap and regulator voltage is constant. This indicates that the regulators are properly working and that the problem is due to the band gap reference. A further irradiation is planned to verify proper operation of the regulators.

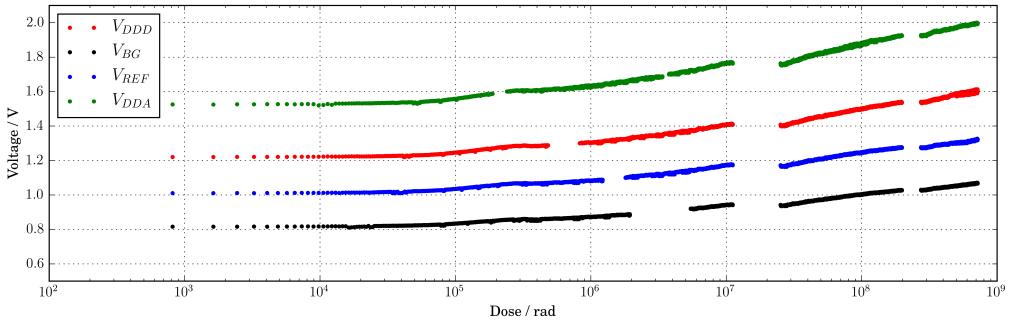

Figure 5: Measured voltage of the regulators and the band gap in the PARC. A read-out inconsistency led to a loss of data which resulted in the depicted gaps.

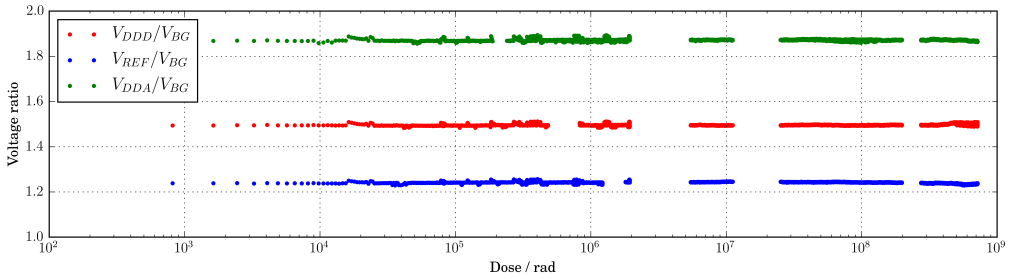

Figure 6: Ratio between the regulator voltages and the band gap voltage.

4. Summary and outlook

A fourth version is designed merging the two chips and correcting the flaws observed with the tests. Temperatures tests below 0 °C will be performed with the next iteration which weren't possible with the climate chamber available. One big change will be the use of bump bonds instead of wirebonds to improve bypass resistance and heat transfer as well as mechanical stability. This will be verified in a magnetic field. We expect to achieve a more robust system than with wirebonds.

The PSPPv3 chip is a working prototype for the new DCS system. It includes all required elements and is already working well. The PSPPv3 will be used together with pixel modules in a system test, where multiple complete serial power chains will be implemented.

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