Design and characterization of the monolithic matrices of the H35DEMO chip

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The H35DEMO chip is a HV/HR-MAPS demonstrator of 18.49 mm x 24.4 mm, fabricated with a 0.35 µm HVCMOS process from AMS in four different substrate resistivities. The chip is divided into four independent matrices with a pixel size of 50 µm x 250 µm. Two of the matrices are fully monolithic and include the digital readout electronics at the periphery. This contribution describes the two standalone matrices of the H35DEMO chip and presents results of the beam tests carried out with unirradiated and irradiated samples with different substrate resistivities.

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1. Introduction

The H35DEMO was the first large area demonstrator fabricated to validate High Voltage/High Resistivity Depleted Monolithic Active Pixels (HV/HR-DMAPS) as a technology feasible for ATLAS pixel detector upgrade foreseen for the High-Luminosity LHC phase [1]. This technology is currently being considered for the outermost (fifth) pixel layer, which at a radius of 28 cm, will have to sustain a fluence of 1.5e15 n_{eq}/cm^2 (corresponding to 4000 fb^{-1} and including a 1.5 safety factor).

The H35DEMO chip was fabricated with a 0.35 µm HVCMOS process in 4 different substrate resistivities through an engineering run: 20, 80, 200, and 1000 Ω·cm. The ASIC size is of 18.49 mm x 24.4 mm and includes four different independent matrices with a pixel size of 50 µm x 250 µm. The pixels of the matrices, called *analog matrices A* and *B*, includes a charge sensitive amplifier and must be either DC or AC coupled to a FEI4 chip for readout. Both matrices are described in detail in [2]. This paper is focused on the standalone matrices NMOS and CMOS. These include electronics to read out the pixels. The purpose of the H35DEMO is to qualify the technology and not to provide a final device to be used in the detector. For this reason, the readout was done simple, with no buffering and no zero suppression.

2. Sensor

The pixels of NMOS and CMOS matrices are equal and only differ on the analog front-end electronics integrated on-pixel. As mention above, the pixel size is 50 µm x 250 µm. A cross section with the different layers is shown in Figure 1. The sensor is a p-n junction formed by a deep n-well over a high resistivity substrate. The latter is biased through a p-well ring with a negative High Voltage (HV). It is important to note that the deep n-well is divided into 3 in the CMOS matrix in order to reduce the total capacitance of the pixel. In such a case, all 3 wells are connected and biased slightly below the analog power supply VDDA (3.3V) through a bias circuit. Under these conditions the p-n junction is reverse biased. Depletions depths of more than 100 µm can be generated depending on the negative HV and the substrate resistivity [3].

It can be seen from Figure 1 that the bulk of p channel transistors is connected to the deep n-well which is the collecting electrode. This forbids the integration on pixel of CMOS circuits as comparators and digital gates because they generate peak currents due to large voltage swings. Noise may be induced to the collecting electrode and hence disturb the response of the sensor. For this reason, the pixel digital front-end electronics are placed at the periphery of the matrix. Comparators can be integrated on pixel only
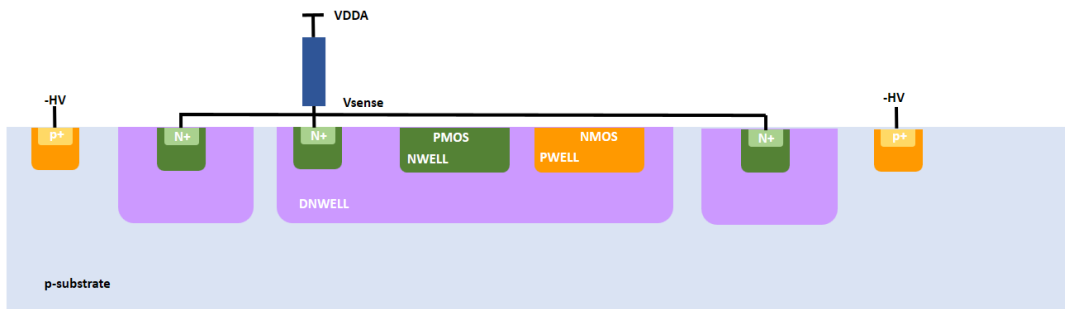

Figure 1: Cross section of a pixel of the CMOS matrix.

if are made of n channel transistors. This was done in the standalone NMOS matrix, which has two pixel flavors. Half of the pixels include a regular NMOS discriminator and the other half a NMOS discriminator with time walk compensation. The output voltage levels of both discriminators are not CMOS, and they need to be translated in order to be processed by digital electronics. A CMOS discriminator placed at the periphery translates the voltage levels. The pixels of the CMOS standalone matrix do not include an on-pixel discriminator. This is placed at the periphery with the rest of the digital readout electronics.

3.   H35DEMO standalone matrices

The standalone pixel matrices are composed of 16 rows and 300 columns. As mentioned above, the main difference between them is the inclusion or not of an on-pixel discriminator. The digital front-end electronics are the same. Each pixel has associated a digital readout cell (ROC) placed at the periphery which function is to process the response of the analog stage. In case of detecting a hit, the cell stores the time stamp corresponding to that event and asserts a hit flag. The ROC cells are arranged in 120 columns of 40 rows which means that 2.5 pixel columns are connected to one ROC column. Such arrangement was needed due to the ROC cells size, 125 µm x 20 µm. The ROCs are divided into two blocks of 40 rows and 60 columns.

A block diagram of the front-end electronics of both standalone matrices is shown in Figure 2. The analog stage is mainly composed of bias circuit, charge sensitive amplifier (CSA) with a constant current discharging circuit, shaper and NMOS discriminator for the NMOS matrix and a second amplifier for the CMOS matrix. The output of the NMOS and CMOS pixels is transmitted to its associated ROC. A CMOS comparator translates the voltage levels of the on-pixel discriminator for the NMOS matrix and determines if there is a hit or not for the CMOS matrix. A 4-bits DAC connected to the discriminator allows to fine tune the global threshold voltage V_{th} locally in order to compensate the input voltage offset. The output of the
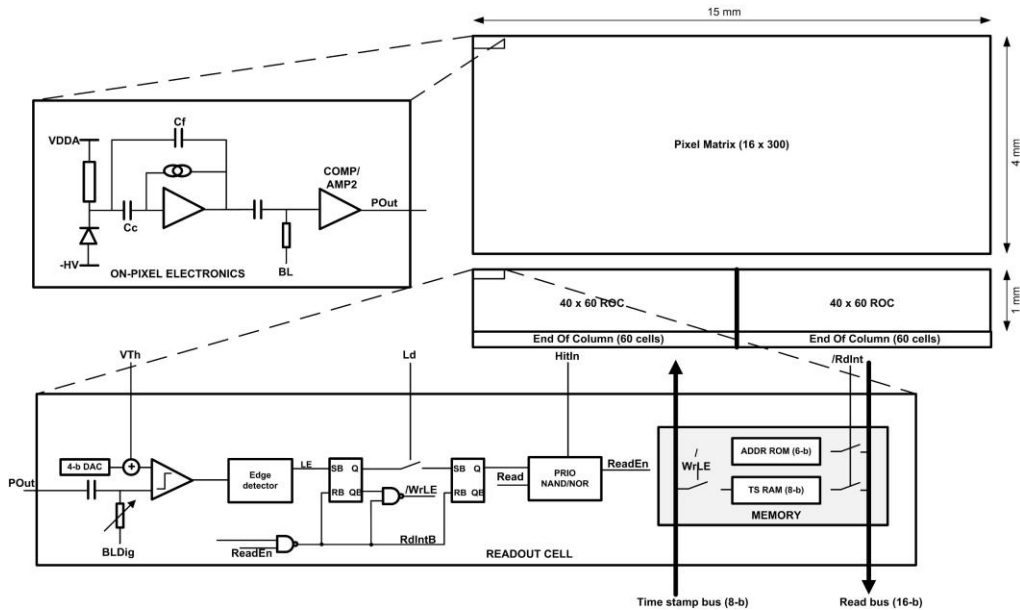

Figure 2: Block diagram of the analog and digital front-end electronics of each pixel. Analog front-end electronics are integrated on pixel, and the digital electronics at the periphery.
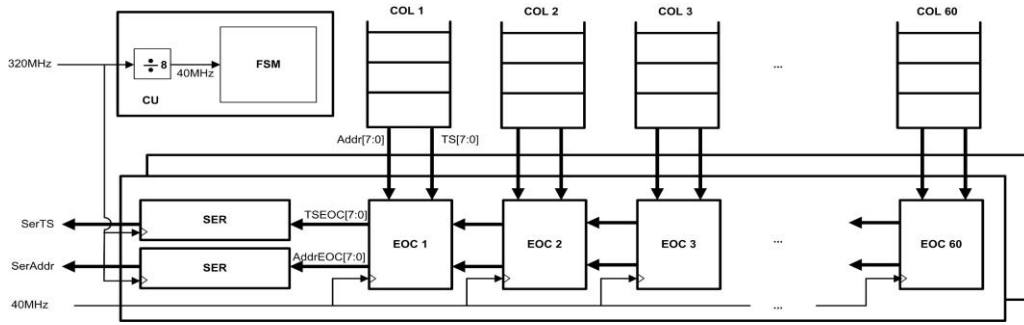
Figure 3: Block diagram of the readout electronics.

discriminator is monitored by an edge detector. When a positive edge is detected, the signal /WrLE is asserted and an 8-bits time stamp is stored into a dynamic memory. A hit flag is also asserted to indicate that a hit has been detected. No new hit is processed until the pixel is read. The address of the pixel is stored into an 8-bit ROM memory.

The architecture of the ROC cell is column drain. The hit flags of the ROC in a column propagate through and NAND-NOR priority chain. As a result, the ROC with the highest address and asserted hit flag has the higher priority.

The stored time stamp and the address is accessed through a 16-bits bus shared by all the pixels in a column. The bus lines are terminated with pull down transistors placed at an End Of Column (EOC) cell. This stores the information into two 8-bit registers which are read/write in parallel. The EOC are connected in such a way that form two 16-bit parallel shift register of 60 elements each one, as show in Figure 3, one for each block of 40 x 60 ROC cells. The two 8-bits outputs of each shift register are connected to two serializers.

The readout process of the matrix is carried out by a control unit. It receives a 320 MHz external clock which is feed to the 4 serializers and to a clock divider. The latter generates a 40 MHz clock used to readout the matrix. The control unit has a 8-bit time stamp generator and finite state machine that generates all control signals for the readout. It executes an infinite loop which consists on 2 steps. In the first one the address and the time stamp of the pixel with the hit flag asserted and with the highest priority in the column are stored in the EOC. If there is no hit in the column zeros are stored. This step is carried out in 1 clock cycle (40 MHz). In the second step, the data stored in the EOC cells is shifted and serialized. When the content of the 60th EOC is being been serialized, new data is stored in the EOC and the loop starts again.

4.   Beam test results

The CMOS matrix of H35DEMO chips have been characterised at the Fermilab Test Beam Facility (FTBF) using a proton beam of 120 GeV. A 6 plane telescope provided by the University of Geneva and made of ATLAS FE-I4 detectors was used for particle tracking. The monolithic matrices of the H35DEMO were operated thanks to a DAQ system developed at IFAE [4].

The efficiency of not irradiated samples of 20, 80, and 200 substrate $\Omega \cdot$cm resitivities was measured as a function of the bias voltage (Vbias). Results are shown in Figure 4.a. Samples with resistivities of 80 and 200 $\Omega \cdot$cm presented an efficiency of more than 99 % for Vbias >= 50V. As expected due to the thinner depletion regions, the samples with the lower resistivity of
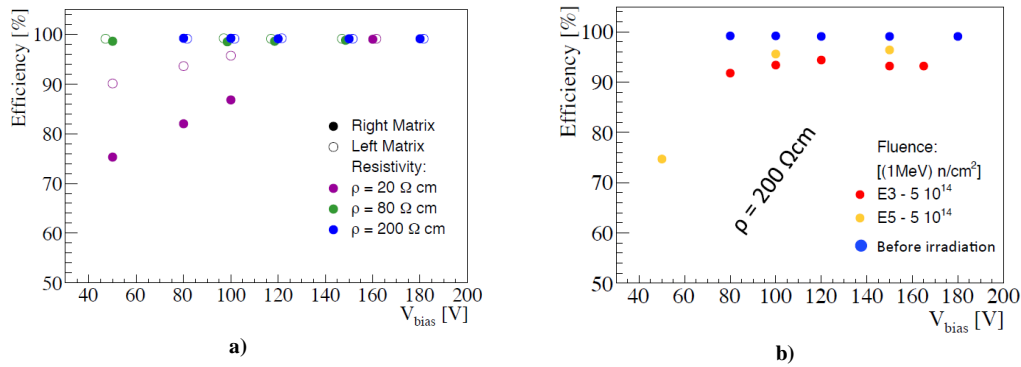
Figure 4: Measured efficiencies for unirradiated samples (a) and irradiated samples (b).

20 $\Omega \cdot$cm required instead a Vbias larger than 150 V to achieve the same performance. Differences in the results of the left and the right part of the matrix are due to different comparator settings. The two sides of the matrix share the same global registers for the tuning of the off-pixel comparators, but have different features for the tuning of trim registers (different number of bits, possibility to turn on/off the trim correction). For this reason it was difficult to optimise the two sides at the same time. In these measurements the right part of the matrix was operated with a larger threshold of the off-pixel comparator than the left part leading to a general lower efficiency.

Very first measurements of 200 $\Omega \cdot$cm samples irradiated with neutrons in the TRIGA reactor of JSI, Ljubljana were also performed in the same test beam campaign. Due to the limited experience with the operations of this chip after irradiation at the time of the measurements, it was possible to extract data only from the right part of the CMOS matrix for two samples irradiated to 5e-14n$_{eq}$/cm^2. The irradiated chips were cooled down between -20 and -30 °C. The results presented in Figure 4.b show efficiencies higher than 90 % for Vbias > 80 V. A more complete characterisation of these chips after irradiation up to the HL-LHC fluences is planned at CERN by the end of this year.

Acknowledgments

References

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