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KLauS4: A Multi-Channel SiPM Charge Readout ASIC in $0.18\,\mu$m UMC CMOS Technology

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KLauS4 is a 7-channel mixed-mode Silicon-Photomultiplier (SiPM) charge readout ASIC dedicated to imaging calorimetry at a possible future linear collider, where one key aspect is the ultra-low power consumption of the readout electronics. The ASIC is designed to read out the SiPM charge information with high precision and over large dynamic range. Each channel consists of a low-noise front-end with two gain branches to deal with a large input signal range, and a 10/12-bit ADC to digitize the charge information; a common digital part for data storage and transmission is also implemented into this chip. Design of the ASIC, characterization measurements and beam-test results will be presented.

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1. Introduction

An imaging calorimeter system is planed to be operated at future linear collider experiments with high spatial granularity to provide the capability of track reconstruction by applying the particle flow algorithm [1]. For such a system the analog hadron calorimeter (AHCAL) of the CALICE collaboration is being developed, whose technology is based on organic scintillator tiles read out by silicon photomultipliers connected to highly integrated readout electronics. Due to the dense structure and no extra space for active cooling, the readout ASICs are required to dissipate not more than 25 μW per channel when being power pulsed with a 1% duty cycle.

The KLauS4 chip is a 7-channel mixed-mode SiPM readout prototype dedicated to this application. Figure 1 shows the block diagram of a single channel. The analog front-end is designed to achieve a sufficient signal-to-noise ratio for single pixel signals of SiPMs with low intrinsic gain, while allowing charge measurements for the full sensor dynamic range [2]. A current conveyor structure is used for the input stage to lower the input impedance and a DAC is implemented in this stage to tune the bias voltage at the input terminal. Two branches for charge integration with different gains are implemented: a high-gain (HG) branch for single pixel signals mainly required for SiPM gain calibration and a low-gain (LG) branch spanning the large charge range. An automatic gain-selection is included to determine which gain branch to be digitized. In addition, a triggering circuit is integrated in the chip to generate a digital time stamping signal with a sub-nanosecond resolution and then digitized by a TDC with 25 ns bin-size. The trigger is also used to initiate the ADC conversion after certain amount of delay configured by the *Hit Logic* circuitry.

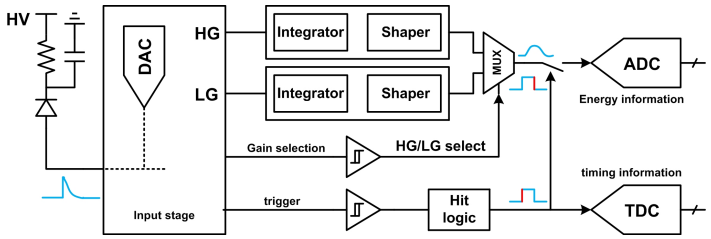

Figure 1: Channel block diagram of KLauS4

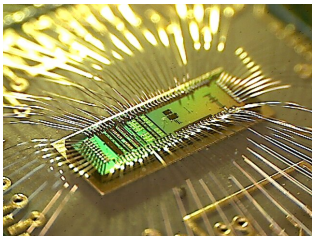

Figure 2: KLauS4 chip

The amplitude of the output signal from the front-end is digitized by an ADC to get the charge information. A 10-bit Successive-Approximation-Register (SAR) ADC is adapted to minimize the power consumption. To measure the single pixel signal from SiPMs with intrinsic gain as low as 10^5 p.e./ph., an addition pipelined SAR stage is implemented to increase the quantization resolution to 12-bit. Detailed description of the ADC can be found in [3].

In order to achieve the ultra low power consumption required by the AHCAL detector, a power gating scheme has been implemented to turn off the ASIC when no bunch is crossing in the beam [1, 2]. During the off state in the power cycle, the input stage works in the sub-threshold region to sustain the DC voltage at the input terminal, while other part of the front-end, the ADC and the digit part are completely turned off.

Figure 2 shows the picture of KLauS4 chip bonded on a test-board. Detailed characterization measurements and the beam-test have been carried out.

2. Measurement results

2.1 Charge readout performance

In order to characterize the charge readout performance of the ASIC, defined charge signals generated by a pulse generator and a capacitor are injected into the input stage. The linearity and noise performance are measured.

The amplitudes of the output signal as a function of the injected charges are measured for the two branches separately. The internal 10-bit ADC is used for this characterization. A linear fit is used to determine the charge conversion factor $\Delta V_{out}/\Delta Q_{in}$ as well as the linear range for a maximum integral non-linearity (INL) of 1% full scale range (FSR). A full-chain linear range of 2.3 pC and of 130 pC is achieved for the HG and LG branch, respectively.

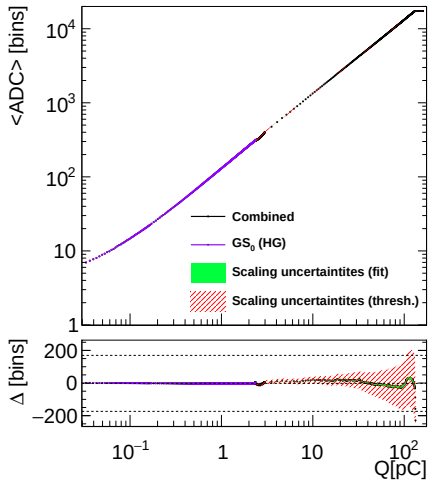

Figure 3: Output amplitude versus injected charge in Auto-gain selection mode

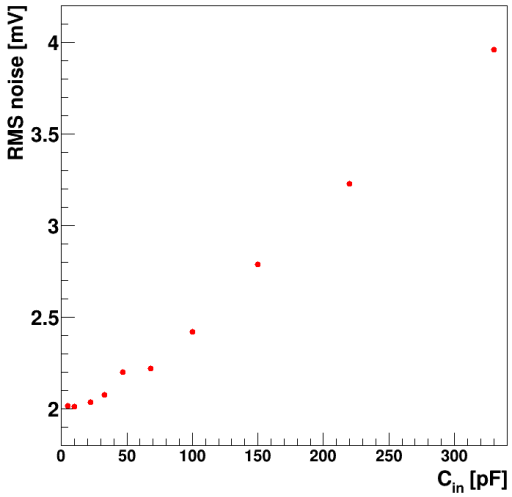

Figure 4: RMS value of the pedestal voltage for the HG branch using only the front-end

In the auto-gain mode, when the input charge is less than the configured threshold, the HG branch is digitized and a flag of '0' is given by the branch-selection comparator; otherwise, the LG branch is selected and a '1' flag is marked. Linearity in the auto-gain selection mode was also characterized by the charge injection measurement. Results from two branches are combined as follows: after subtracting the pedestal value of the respective branch, the digital codes from the HG branch are mapped directly to the combined results, while those from LG branch are multiplied with an inter-calibration gain. As shown in Figure 3, linearity of the combined result is satisfying and a total linear range of 130 pC is well preserved in the auto-gain mode.

The noise performance has also been characterized by measuring the RMS value of the pedestal voltage, as depicted in Figure 4. The equivalent noise charge (ENC) for the HG branch is measured to be smaller than 6 fC for input capacitance less than 100 pF. The measurements also suggest that the noise contribution from front-end is dominant.

2.2 Power pulsing functionality

For a stable operation of the SiPM sensor, it is important that the power cycling does not affect the bias voltage at the input terminal [4]. Figure 5 depicts the waveform of the input terminal within

a power cycle. The voltage difference between *on* and *off* states is measured to be less than 20 mV for all DAC configurations. This corresponds to less than 1% of the 2 V tuning range of the SiPM input bias voltage and thus can be neglected.

Another important parameter for the ASIC is the setup time after power on during the power pulsing. Since the ADC and digital part can response relatively fast, the time needed for recovery of the front-end is critical and is measured to be less than 10 μs. Based on this result, the duty cycle can be reduced from 1% to smaller value close to 0.5%, which could further cut down the average power consumption of the ASIC.

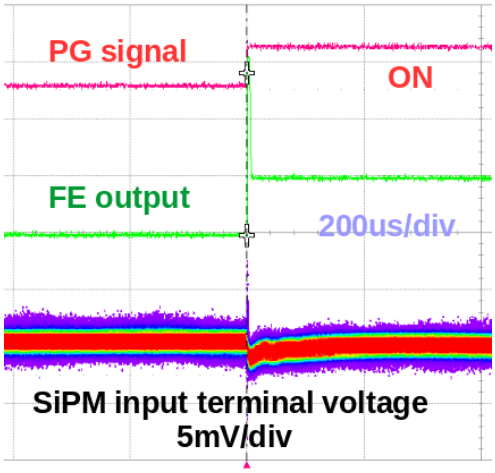

Figure 5: Waveform of the FE output and SiPM input terminal during power pulsing

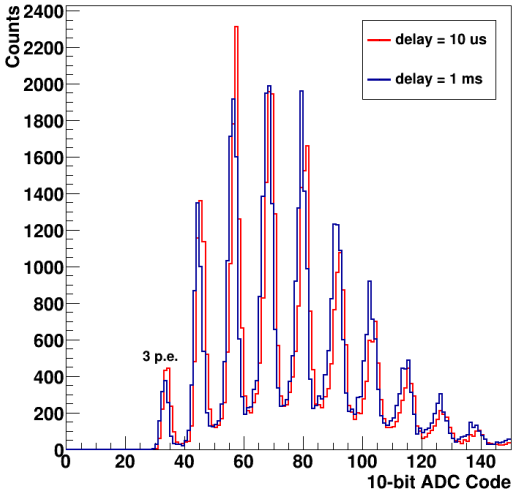

Figure 6: SPS with different time delay between turning on the ASIC and the illumination of the SiPM

The readout of Hamamatsu S10362-11-25C MPPC with power pulsing is shown in Figure 6. The amplitudes of the charge signals with different time delay between turning on the ASIC and the illumination of the SiPM are measured. The single photo spectra (SPS) from time delay $\Delta t = 10\,\mu$s and $\Delta t = 2$ ms are compared without observable difference between the locations of the photo-peaks. This again indicates that the ASIC works well with a time delay less than 10 μs after being switched on during power pulsing.

2.3 Beam-test results

Test measurements were also carried out at the DESY test-beam facility on February 2017. A three-layer setup comprised of scintillator tiles, Hamamatsu S13360-1325PE MPPCs and KLauS4 ASICs was constructed. Two layers were fully equipped for all 7 channels, while the other layer was equipped only for one channel. The three layers were arranged in a row perpendicular to the beam direction.

The multi-channel operation could be verified by recording minimum ionization particle (MIP) spectra in all of the equipped channels. Figure 7 shows the MIP spectra recorded in the 5.6 GeV electron beam. The one-MIP signal is clearly measured and dominate the spectra. Two additional small peaks correspond to two-MIPs and three-MIPs signals due to the particle shower. Spectra with and without power pulsing is also compared and shows no displacement of the MIP peaks.

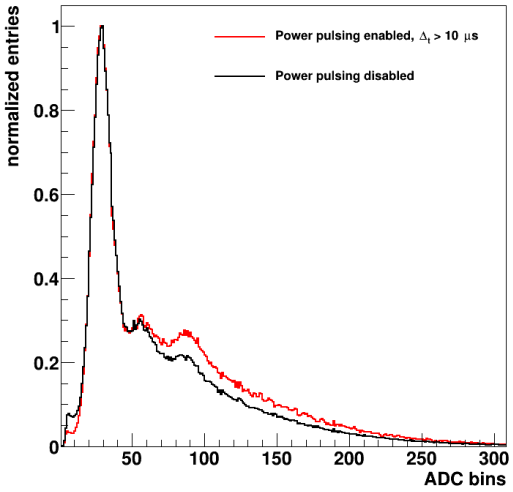

Figure 7: MIP spectra recorded in the test-beam with and without the power pulsing

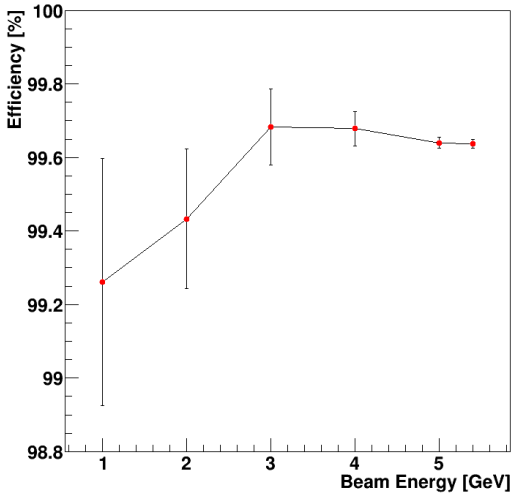

Figure 8: Detection efficiency at different beam energy

Detection efficiency of the setup was also tested for different beam energy setting. In this measurements, coincidence of the center channel in the two outer layers is identified as a particle transverses the center scintillators of all layers. The efficiency of the same channel in the center layer is measured. As it shown in Figure 8, the efficiency is larger than 99%. Other functionalities such as auto-gain selection were also verified and showed very satisfying results.

3. Conclusion

The mixed-mode KLauS4 ASIC has been developed in the 0.18 μm CMOS technology and provides a readout solution for SiPMs used in the scintillator based analog hadronic-calorimeter. The ENC is measured to be smaller than 6 fC and thus ensure the measure for SPS of SiPM with low intrinsic gain. The dynamic range for the LG branch is 130 pC. The ASIC can work well 10 μs after being switch on during power pulsing. Beam test has also been carried out and the results are promising. All the measurements showed that the KLauS4 ASIC fulfills the severe constraints of the AHCAL detector design. A 36-channel prototype has been submitted in July 2017 and is foreseen to be used in the AHCAL technical prototype.

References

[1] T. Behnke et al., *The International Linear Collider Technical Design Report - Volume 4: Detectors* (2013)

[2] K. Briggl et al., *KLauS: a low power Silicon Photomultiplier charge readout ASIC in 0.18 UMC CMOS*, 2016 *JINST* **11** C03045.

[3] W. Shen et al., *A dedicated Analog-to-Digital-Converter for Silicon Photomultiplier Readout*, *IEEE NSS/MIC 2014*

[4] T. Harion et al., *KLauS - A Charge Readout and Fast Discrimination Readout ASIC for Silicon Photomultipliers*, *IEEE NSS/MIC 2012*