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Development of a Front-End ASIC for 1D Detectors with 12 MHz Frame-Rate

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We present a front-end readout ASIC developed for a new family of ultra-fast 1D imaging detectors operating at frame rates of up to 12 MHz. The ASIC, realized in 110 nm CMOS technology, is designed to be compatible with different semiconductor sensors. The final chip will contain up to 128 channels, each consisting of a Charge-Sensitive Amplifier, a noise shaper based on a fully-differential Correlated Double Sampling stage and a Sample-and-Hold buffer. The differential channels are connected through 8:1 analog multiplexers to the output drivers, which directly interface external analog-to-digital converters. A first prototype with a limited number of channels have been characterized with a Si microstrip detector. When operated at the maximum frame-rate of 12 MHz, the ASIC exhibits an Equivalent Noise Charge of 417 electrons with a detector capacitance of 1.3 pF.

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1. Introduction

KALYPSO is a line scan detector developed for ultra-fast beam diagnostics for several accelerator facilities [1]. The main features of KALYPSO are the high frame-rate and the continuous data acquisition, thus enabling the monitoring of different proprieties of the particle beam at the repetition rate of the accelerator. The current version of KALYPSO is based on a modified version of the GOTTHARD chip [2, 3], which operates with a maximum frame-rate of 2.7 MHz. With respect to the previous GOTTHARD chip, some functions (*e.g.* the automatic gain-switching stage) have been removed and the overall power budget has been re-allocated across the different analog stages to increase the analog bandwidth. However, an even higher frame-rate is required to meet the experimental requirements of different accelerators (*e.g.*, the European XFEL operates with a repetition rate of 4.5 MHz). To further increase the frame rate, a dedicated readout Application Specific Integrated Circuit (ASIC) is being developed for the final version of the KALYPSO detector system. In this paper, the design and the characterization of the first prototype will be described. The prototype, designed in a 110 nm CMOS technology from UMC, features 48 channels with a 50 µm pitch and operates with a continuous frame rate of 12 MHz at full occupancy. In the final version of the ASIC the number of channels will be increased to 128, and several chips will be connected to a microstrip sensor with up to 2048 channels.

2. Detector architecture

An overview of the front-end electronics of the KALYPSO system is shown in Figure 1. The different channels of the readout ASIC are connected to a microstrip sensors, which is chosen according to the experimental requirements. To be compatible with different types of Si or InGaAs microstrip sensors, the chip must be able to process signals of both polarities with a detector capacitance up to 6 pF. Each readout channel consists of a Charge-Sensitive Amplifier (CSA), a noise-shaping stage and a channel buffer. The ASIC is mounted on a FPGA Mezzanine Card (FMC) together with commercial Analog-to-Digital Converters (ADC) and additional components such as clock conditioners and voltage regulators. The digitized values are acquired by the FPGA readout card, which also synchronizes the operation of the ASIC with the accelerator timing system.

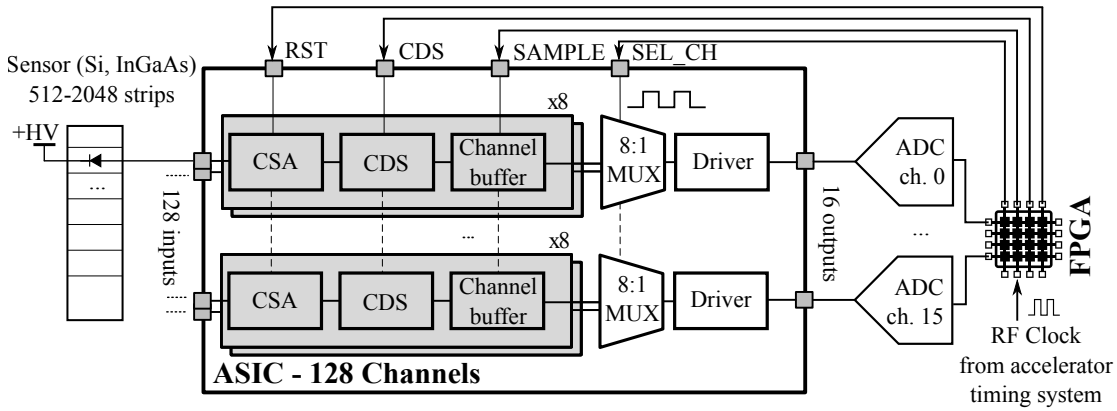

Figure 1: Block diagram of the readout ASIC and the KALYPSO front-end electronics.

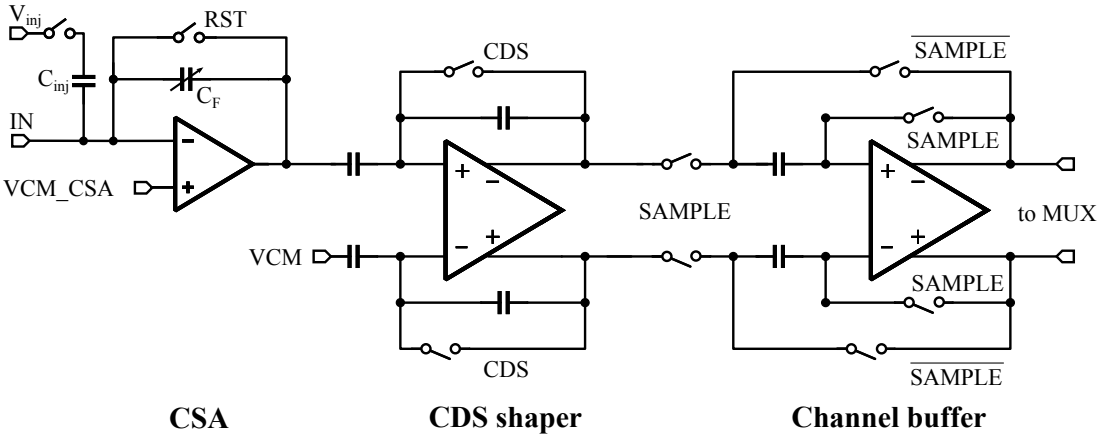

Figure 2: Simplified schematic of one readout channel.

3. Design

The CSA is implemented as a differential folded-cascode amplifier with a variable feedback capacitance and a synchronous reset. The folded architecture has been preferred because of its high gain-bandwidth product, stability and output swing. Despite the higher intrinsic noise of a differential architecture with respect to single-ended amplifiers, the differential architecture ensures a high rejection of external noise sources. This is a critical aspect for this development, because the readout ASIC will be closely integrated with noisy components such as FPGAs, PCI-Express data links and the accelerator timing distribution system. Thus, a differential architecture ensures proper operation in all scenarios and eases the system level design at the cost of a higher ENC. A test pulse capacitance C_{inj} has been implemented on-chip to inject a known charge at the input of the CSA to evaluate the performance of the readout chain. However, the injection capacitance has been implemented only in certain channels, while the neighboring channels are left disconnected. This allows us to evaluate the cross-talk between different channels due to the electronics, as will be described in the next section.

The shaper performs Correlated-Double-Sampling (CDS), reducing the low-frequency and kT/C noise introduced by the synchronous reset mechanism [4]. In order to achieve high frame-rates, a sample-and-hold channel buffer is necessary to allow *integrate-while-read* operation. The timing strategy for a frame-rate of 10 MHz is shown in Figure 3. The different readout phases are controlled by the `RST`, `CDS` and `SAMPLE` signals, which are generated by the FPGA. Dedicated on-chip circuitry generates the correct timings for the switched capacitor circuits, as described in [5].

The output of each channel is connected through an analog multiplexer (MUX) to a high-speed I/O buffer, which drives the external ADC with a settling time below 4 ns. During the hold phase, the signal at the output of the channel buffer is digitized by the external ADC. To cycle through all the channels connected to the analog MUX in a single readout cycle, the switching frequency of the MUX must exceed 100 MHz. Thus, the channel buffer has been optimized for fast settling times. To optimize the bandwidth while ensuring proper performance under PVT variations[1], a

[1]Process, temperature and power supply voltage.

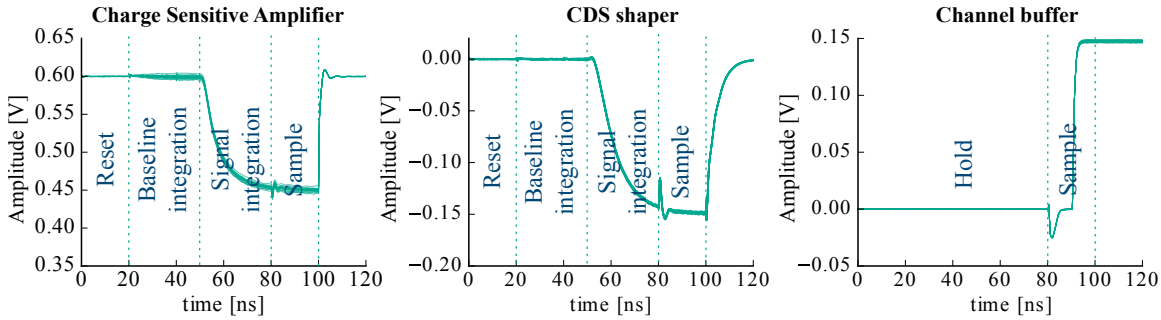

Figure 3: Simulated response of the CSA (left), the CDS (middle) and the channel buffer (right) to a signal of 5 fC and a detector capacitance of 1.3 pF. For simplicity, the different readout phases and their duration are shown for a 10 MHz frame-rate operation. A 12 MHz frame-rate can be achieved by reducing the duration of each phase. Different traces obtained through Monte Carlo transient noise simulations are superimposed on the plot, to highlight the "reset noise", *i.e.* the noise introduced after the `RST` is released.

two-stage architecture with cascode compensation has been adopted [6]. To achieve high speed and low distortion with a 100 Ω load, the output driver has been designed with a two-stage class-AB OpAmp with cascode Miller compensation and Monticelli biasing scheme [7]. This last stage drives large capacitive off-chip loads, with a settling time of less than 4 ns and a non-linearity error of around 0.5% over a dynamic range of ±900 mV.

4. Performance

The prototype of the ASIC has been mounted on a dedicated FMC board, which is shown in Figure 4. The design of the FMC board is similar to the one of the final version of the KALYPSO detector system, therefore the ASIC has been characterized in the final experimental environment. The chip operates with a power-supply voltage of 1.2 V and a power consumption of 1.7 mW/channel (including the high-speed output drivers). A gain of 37 mV/fC and an Integral Non-linearity (INL) error of less than 1% for the highest gain setting have been measured, as shown in Figure 5. The ENC has been evaluated by injecting a known charge through the test capacitance

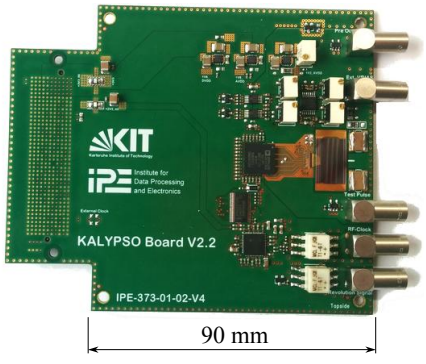

Figure 4: Picture of the FMC board used to characterize the ASIC.

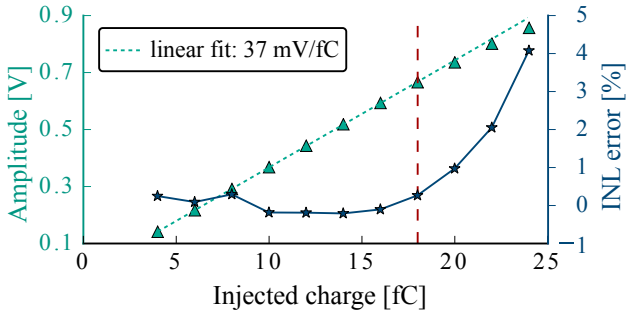

Figure 5: Measured transfer curve of the ASIC with the highest gain setting and INL error of the full analog chain. The CSA shows signs of saturation for input signals above 17 fC.

C_{inj} and by measuring the noise at the output. When connected to a Si microstrip detector with a pitch of 50 µm and a detector capacitance of 1.3 pF, the ENC is 417 $\pm$ 25 electrons, in agreement with the results obtained by post-layout simulations. At the moment of writing, the characterization of the ASIC with other sensors, such as an InGaAs *p-i-n* photodiode array, is ongoing.

The ASIC has been disconnected from the microstrip sensor to evaluate its performance in terms of cross-talk and output driving capability. A large signal is produced in a few selected channels through C_{inj} and the output of the neighboring channels is recorded. If the settling time of the signal at the output driver is not sufficient to load the input stage of the external ADC within a sampling period, a significant cross-talk would be observed between two consecutive channels. Therefore, the MUX is operated at the maximum switching frequency[2] of 125 MHz, which results in a frame-rate of 12 MHz. A cross-talk of less than 0.5% has been measured.

5. Conclusion

The first prototype of a novel readout ASIC for the KALYPSO detector has been presented. The chip has been successfully tested and characterized, and its performance meets the design specifications. We are currently evaluating the possibility of replacing the CDS noise shaper with a trapezoidal time-variant shaper, in order to further optimize the noise performance of the chip [8]. The production of the final version of the readout ASIC with 128 channels and the integration with the final version of the KALYPSO detector system are planned for the first months of 2018.

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[2]The maximum switching frequency is limited by the maximum sampling rate of the AD9681 ADC mounted on the FMC board