

# A Low-Noise CMOS Pixel Direct Charge Sensor Topmetal-IIa for Low Background and Low Rate-Density Experiments

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We present the design and characterization of a CMOS pixel direct charge sensor, Topmetal-IIa, fabricated in a standard 0.35 $\mu\text{m}$  CMOS process. The sensor features a  $45 \times 216$  pixel array with a 40 $\mu\text{m}$  pixel pitch which collects and measures external charge directly through exposed metal electrodes in the topmost metal layer. Each pixel contains a low-noise charge-sensitive preamplifier to establish the analog signal, which is read out through time-shared multiplexing over the entire array. Compared to the earlier Topmetal-II- chip, the analog readout noise of Topmetal-IIa is reduced by 10.8% from 13.9e<sup>-</sup> to 12.4e<sup>-</sup>, and the DC voltage variation noise is reduced by 21% from 1.2mV down to 0.946mV. The sensor is capable of detecting both electrons and ions drifting in gas. These characteristics enable its use as the charge readout device in future Time Projection Chambers without gaseous gain mechanism, which has unique advantages in low background and low rate-density experiments.

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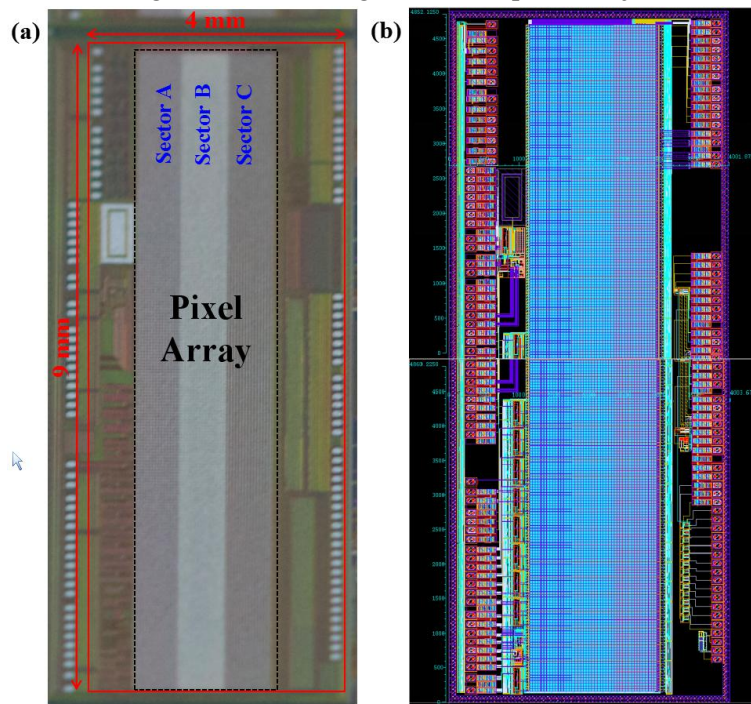
## 1. Introduction

With the development of nuclear and particle physics, the low background (low event-rate density and low charge drifting speed) and low noise experiments are developed as research mainstream and hot spots in the future high energy physics experiments. Notable examples are neutrinoless double beta decay ( $0\nu\beta\beta$ ) [1] and dark matter searches. Gaseous or high pressure cryogenic liquid Time Projection Chambers (TPCs) [2] have been considered as ideal detectors for the low-background and low-noise experiments. Therefore, sensors with low-noise, high pixel density and high integration can be satisfied with the requirements of future high energy applications.

We designed a CMOS IC, Topmetal-IIa, that is aimed at direct-charge collecting and measuring in TPCs without gas-avalanche gain. It is a highly pixelated sensor with  $40\mu\text{m}$  pitch between  $45 \times 216$  pixels fabricated in a standard  $0.35\mu\text{m}$  CMOS technology without post-processing for direct charge collection and imaging through exposed metal electrodes in the topmost metal layer. Each pixel contains a low-noise charge-sensitive preamplifier to establish the analog signal, which is read out through time-shared multiplexing over the entire array. Compared to our earlier Topmetal chip, Topmetal-II- [3], this one realizes better noise performance as expected. In this paper we present the overall design and some preliminary test results of Topmetal-IIa. Further test results and relevant applications will be presented elsewhere.

## 2. Sensor structure and operation

A photograph of one fully fabricated Topmetal-IIa sensor is shown in Fig. 1 (a). The sensor is implemented in a  $4 \times 9 \text{ mm}^2$  (red box) silicon real-estate area. With  $40\mu\text{m}$  pitch distance between pixels, the  $45 \times 216$  pixel array makes up a  $1.8 \times 8.64 \text{ mm}^2$  (dashed box) charge sensitive region. The overall layout of the sensor is shown in Fig. 1 (b). Peripheral circuits including readout interface logic and two analog buffers are placed adjacent to the pixel array.



**Figure 1:** Photograph of a Topmetal-IIa sensor (a) and its overall layout (b)

## 2.1 Pixel structure and readout

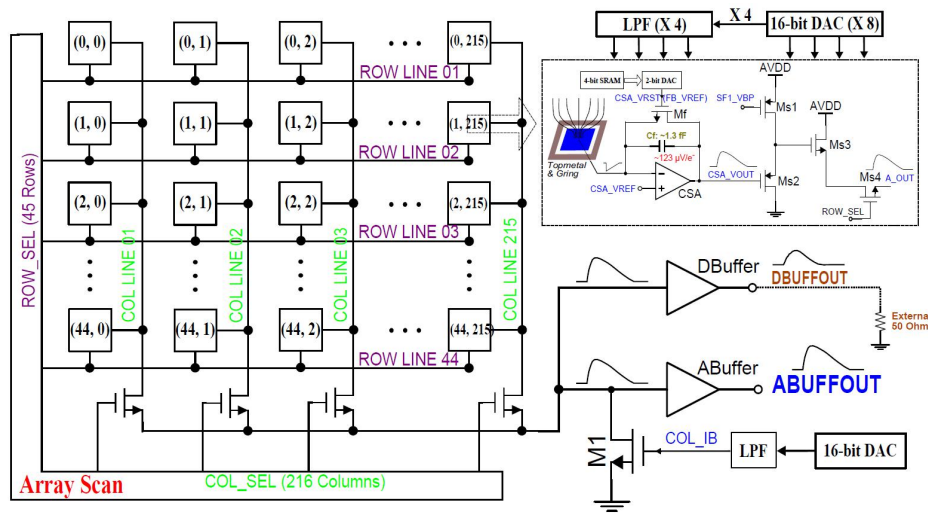
The inner structure of the signal pixel and the analogue readout pathway are shown in Fig. 2. The implementations of the charge collection electrode and a time-shared analog multiplexing structure have been validated in Topmetal-II-. Here we will mainly focus on the following improvements and optimizations over Topmetal-II- chip:

- Based on the CSA's generic noise model [4], for the Topmetal sensor, the total Equivalent Noise Charge (ENC) of CSA:

$$ENC^2 = (C_{in} + C_f)^2 \left( \frac{a_1 4kT\gamma}{g_m \tau_c} + \frac{a_2 K_f}{C_{ox}^2 WL} \right) + \frac{a_3 4KT\tau_c}{R_p}$$

Where  $C_f$  is the feedback capacitor that is reduced to 1.3fF in order to realize higher charge conversion gain ( $1/C_f = 123\mu\text{V}/e^-$ ) hence to improve the signal-to-noise ratio.

- A 2-bit in-pixel DAC is applied to the gate node of the feedback transistor of the CSA, in order to calibrate the total mismatch of the devices, hence improving the CSA's peaking and decay time uniformity.
- CSA's sensitive voltage biases that have significant contributions to the output noise are individually provided by the peripheral Low-Pass Filter (LPF) with tunable cut-off frequency, aiming to improve the noise performance.
- Added an analog buffer (DBuffer) that is capable of 50Ohm driving strength aiming to eliminate the external buffer hence reducing the entire readout system noise.



**Figure 2:** Inner structure of the signal pixel and the analogue readout pathway

The analog signal from each pixel is read out through the traditional “rolling shutter” style time-shared multiplexer controlled by the array scan unit, and then is fed to two array-shared analog buffers. For its intended application, event-rate density is expected to be low and charge (both free electron and ion) drifting speed is expected to be slow; therefore, we tuned the CSA to have long signal retention and eliminated the in-chip pulse shaper while focusing on improving the noise performance.

## 2.2 Simulation results

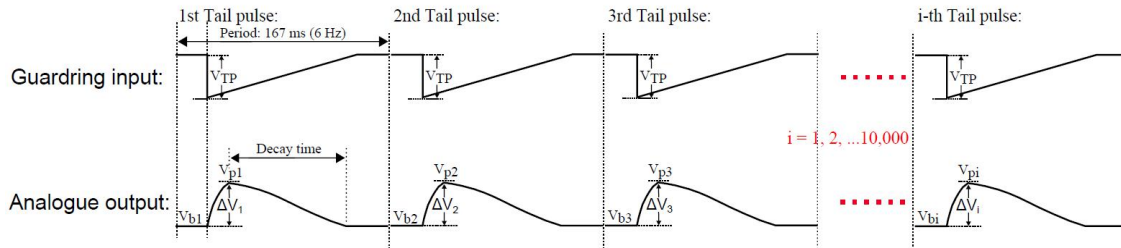
The full process-corner post simulation results (Signal response and Noise) of a typical  $3 \times 3$  Pixel Array Readout are summarized in Table 1. The Equivalent Noise Charge of the sensor is around  $10e^-$  rms at  $1000e^-$  injected charges and with a detector capacitance of 11.5fF.

Process corner	Temperature [°C]	Signal response			Noise	
		Amplitude [mV]	Rising time [μs]	Decay time [ms]	rmsNoise [mV]	ENC [e <sup>-</sup> ]
tm	0	99.7	4.1	110	0.963	9.66
	27	96.9	13.3	99	0.808	<b>8.18</b>
	85	96.1	<b>28.3</b>	8.8	<b>1.513</b>	<b>15.76</b>
wp	0	<b>100.7</b>	6.4	128	0.973	9.66
	27	97.9	4.8	106	0.973	9.93
	85	100	3.6	<b>4.5</b>	1.339	13.39
ws	0	86.4	6.2	<b>151</b>	0.989	11.44
	27	83	7.8	115	0.824	9.92
	85	<b>81.4</b>	<b>5</b>	7.9	<b>0.74</b>	9.08
MIN		81.4	5	4.5	0.74	8.18
MAX		100.7	28.3	151	1.513	15.76

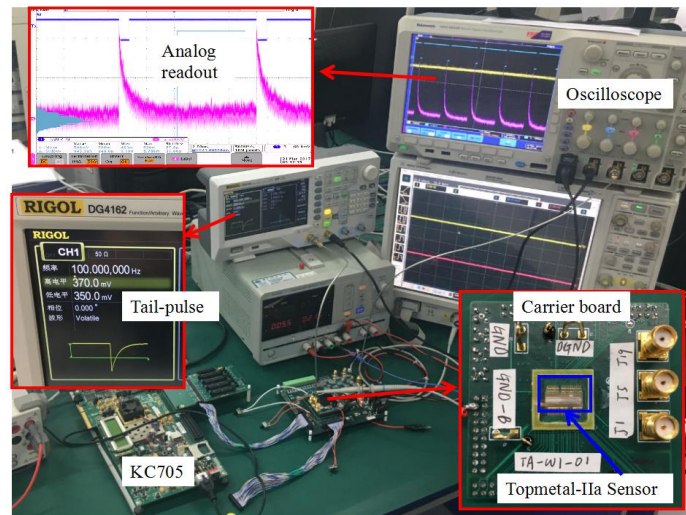
**Table 1:** Simulation results of 3 × 3 Pixel Array Readout (@ $Q_{in} = 1000e^-$ ,  $C_{in} = 11.5fF$ )

### 3. Preliminary test results

We applied a repetitive Tail-pulse (see Fig. 3) with an amplitude of 20mV and the frequency of 6Hz on Gring. Since there is a coupling capacitance,  $C_{inj} = 2.04fF$ , at each transition edge of the Tail-pulse, an equivalent charge  $Q_{in} = 20mV * C_{inj} \approx 254.6e^-$  is injected to the CSA. The repetition of the Tail-pulse is 10000, and data acquisition of the analog readout is directly sampled via the DBuffer by the 50Ohm-termination channel of the Oscilloscope. The overall test setup is shown in Fig. 4.



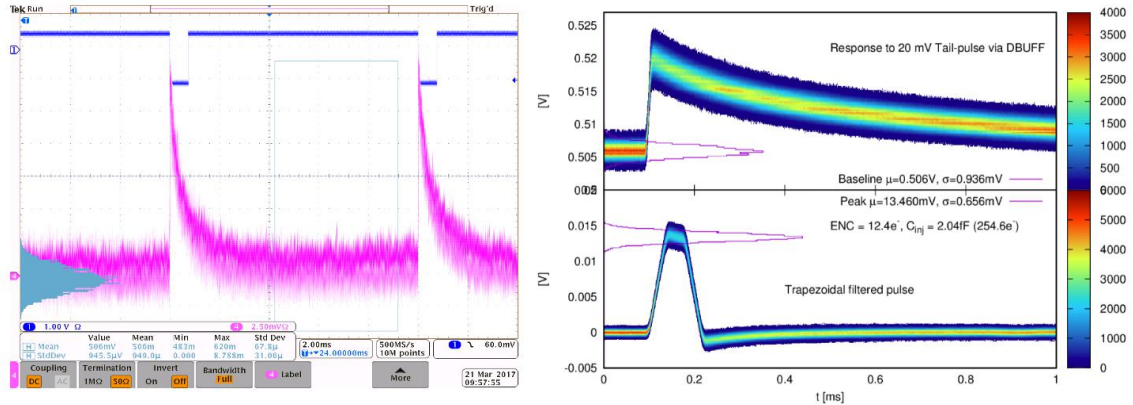
**Figure 3:** External tail-pulse input and Sensor's analogue output



**Figure 4:** Photograph of the overall test setup



Using the pixel selection feature to stop at a fixed pixel and using the Digital Trapezoidal Filter [5] to digitize its analog output continuously. As shown in Fig. 5, the histogram measurement of OSC shows the StdDev of the baseline of the DBuffer output is  $945.5\mu\text{V}$ . By collecting many pulses, the pulse height has a mean value  $\mu = 13.46\text{mV}$ , and a standard deviation  $\sigma = 0.656\text{mV}$ . The ENC is  $Q_{\text{in}} * \sigma / \mu = 12.4e^-$ .



**Figure 5:** Preliminary measurement results of analogue readout noise

#### 4. Summary and Outlook

We present the design and characterization of a CMOS pixel direct charge sensor, Topmetal-IIa, fabricated in a standard  $0.35\mu\text{m}$  CMOS process. Both the simulation and preliminary electrical measurements confirmed the low-noise design. Compared to the earlier Topmetal-II- chip, the analog readout noise of Topmetal-IIa is reduced by 10.8% from  $13.9e^-$  [3] to  $12.4e^-$ , and the DC voltage variation noise is reduced by 21% from  $1.2\text{mV}$  [3] down to  $0.946\text{mV}$ . Based on the simulation results, the analog noise per pixel is expected below  $10e^-$ , thus further more tests and relevant applications are ongoing.

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