PROCEEDINGS OF SCIENCE

A high-Precision Timing ASIC for TOF-PET Applications

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Time-of-flight (TOF) measurement in PET scanners allows a more accurate image reconstruction and/or a lower delivered radiation dose. We are developing a fully custom ASIC to take advantage of the characteristics of the SiGe Bi-CMOS process for timing measurements, integrating a fully-depleted pixel matrix with a low-power BJT-based front-end per channel, integrated on the same 100 µm thick die. All the pixels are multiplexed to a single TDC to extract timing information. Each front-end includes a BJT preamplifier with active feedback, a CMOS discriminator and a calibration DAC. A triggered readout logic is included to reduce the data to be read out of the system. The target timing resolution is 30 ps for a 511 keV photon with a 1 pF input capacitance. The front-end has a gain of ~95 mV fC^{-1} and a rise time of ~1 ns. Its low power consumption of 135 µW, makes it possible to stack multiple ASICs on top of each other, in order to increase the detection efficiency. A total of more than 1 million channels will form the complete scanner. A full-featured prototype with a small 10-by-3 pixel matrix has been submitted in April 2017, after a number of smaller prototypes to validate each block. A full-size chip is currently being designed.

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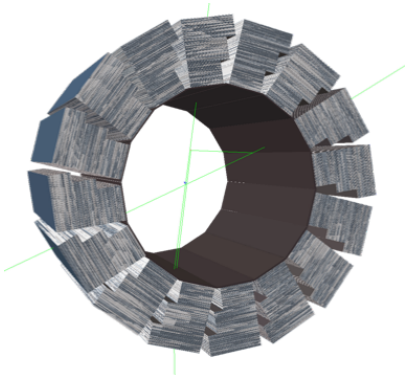

Figure 1: Geometry of the entire scanner

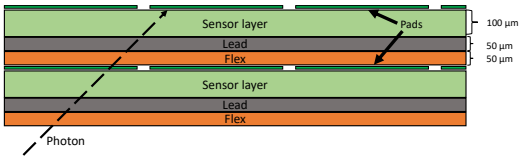

Figure 2: Detection layers stack

1. Motivations

The goal of the TT-PET project[1] is building a high resolution (sub 30 ps) timing scanner for small animal PET imaging. In conventional PET, coincidence detectors are used to determine along which line of response an annihilation has occurred. The information added by the TOF measurement allows a more accurate determination of the position of the annihilation by reducing the line of response to a short segment. In order to extract valuable information on the position of the annihilation point, a high TOF precision is required (at least < 200 ps, but higher resolutions lead to more accurate results). To achieve a good timing performance, front-ends need to have a low equivalent noise and a fast rise time (to reduce the jitter as much as possible).
In order to achieve this result, which is beyond the state-of-the-art for time-of-flight PET scanners[2], a novel approach is used, with a stack of layers of monolithic silicon pixel detectors and high-Z photon-converters. Data is reconstructed off-line to discriminate photon coincidences and reconstruct the acquired image.
The project was funded by the Swiss National Science Foundation and includes multiple institutes across Switzerland and foreign countries. The front-end design is carried out by University of Geneva and University of Rome Tor Vergata, while the readout electronics is being designed by University of Bern.

2. The TT-PET scanner

The scanner is composed of a toroidal structure, 1.3 cm thick and with an inner radius of 2 cm, to be used with mice. It is formed by 16 identical detecting "wedges", placed as in figure 1. The space between the wedges is used for mechanical support and cooling.
The 16 wedges are composed of a stack of 60 detection layers, each composed by a 100 µm monolithic pixel silicon detector, a 50 µm high-Z converter (lead) and a 50 µm flex cable for the interconnection (see figure 2). Pixels have an area of 500 µm by 500 µm, which corresponds to an input capacitance for the Front-end of about 1 pF including routing. The flex cables to all the layers are hierarchically connected to one FPGA per wedge, managing the data acquisition and control of the ASICs.
In order to form the shape of the wedges, there are 3 different chip sizes (they are all 25 mm long

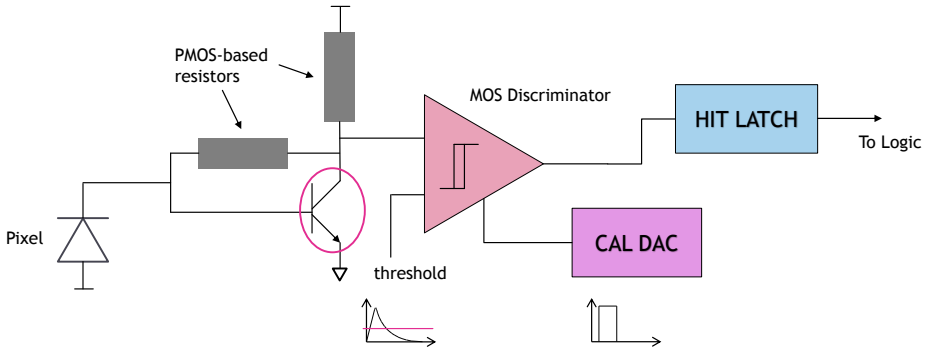

Figure 3: Block diagram of the analog Front-end

and 7, 9 or 11 mm wide), with bigger chips positioned further away from the center of the scanner. The scanner was simulated using both FLUKA and GEANT4 (see [3]). The geometrical acceptance of the scanner was fond to be 85% and the gamma detection efficiency is 25%x for perpendicular tracks. The expected coincidence rate is 3 MHz with a 50 MBq point source. Spurious hits are filtered out using the timing information, with the rate of random coincidences being less than 0.5% of the source activity, calculated using a 1 ns coincidence window.

3. ASIC architecture

3.1 Analog Front-end

In order to achieve a good timing resolution, two main jitter contributions need to be optimized: rise time and signal-to-noise ratio. A first-order evaluation of the timing performance can be written as

$$\sigma_t \cong \frac{t_{rise}}{S/N}$$

ignoring contribution from the digitization, which can be made negligible by using a TDC with a small enough binning. It can be seen (as in [4]) that the main contribution to the front-end noise is the series noise of the input transistor. For this reason the choice of technology fell on Silicon-Germanium Heterojunction Bipolar Transistor technology (SiGe-HBT), which demonstrated[5] the possibility of a sub-100 ps jitter for a 1 pF input capacitance. The signal dynamics in the sensor was simulated using TCAD software and was found to have a negligible contribution to the time resolution compared to the electronics. Although peak values of β and f_T are reached for a current bias of ~1 mA, a good compromise was found for a current of 75 µA, giving better performance than MOSFET devices for the same power consumption.
The pixel analog Front-end is depicted in figure 3. A simple common-source configuration with PMOS-based load and feedback resistors is used, as more complex architectures were found to be generally slower and thus with a worse timing performance. The pulse is then sent to a 3-stage MOS fast discriminator, which can be calibrated with a 7-bit DAC. The digitized signal is then sent to the TDC. Results of simulations performed on the circuit are shown in table 1. It is worth noting that charge collected from 511 keV photons in a PET application is significantly higher than 1 fC, peaking at around 2 fC and with an average of about 3 fC. Since a larger signal corresponds to a

Power supply	1.8 V
Gain	95 mV fC^{-1}
Equivalent Noise Charge	696 e^-
Power consumption	135 µW
Peaking time	1.3 ns
ToA jitter (for a 1 fC signal)	82 ps

Table 1: Main specifications of the simulated analog front-end

larger SNR, the expected average timing resolution is approximately 30 ps.
The ASIC uses a monolithic integration technique to include both the pixel electronics and the sensor diodes in the same substrate. The electronics don't physically sit inside the pixels though, as the sensor area is confined by a guard-ring structure that safeguards the sensitive circuits from the high voltage sensor bias. All the pixels are laid out at the borders of the chip, on the two longer sides, while the chip periphery is on one of the shorter side (see figure 4).

3.2 Digital logic

The outputs of all pixels in a single chip are multiplexed and sent to a single hybrid TDC in the periphery, to digitize time-of-flight and time-over-threshold (to compensate for time-walk). This is possible because the expected hit rate is very low (below 20 KHz per chip[3]), with a 3-hit buffer memory to avoid pile-up issues. At the same time, a position logic extracts the coordinates of the pixel that produced a hit.
In order to minimize the number of connections on the data flex, a daisy-chain communication protocol was used, sending data through multiple chips on a common bus. This limits the number of connection to a bare minimum (clock, data in/out, reset). The readout is performed at 50 MHz over a single serial line per group of 10 chips.

4. First Measurements

A few test chips have been developed so far during the R&D. A first small ASIC with a full Front-end was produced at the end of 2016, while a fully-featured prototype with a 3-by-10 pixel array (its layout is shown in figure 5) has been submitted in April, 2017. Preliminary measurements were performed on the first test chip, which included 11 Front-end channels and two different-sized photodiodes, with the aim of separately studying both the circuit performance and the monolithic integration. The fully-featured prototype testbench is being worked on at the time of writing.

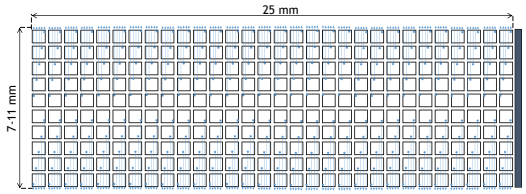

Figure 4: Floorplan of the ASIC

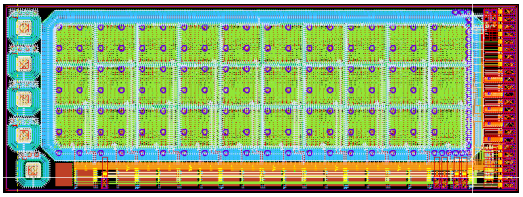

Figure 5: Layout of the ASIC prototype

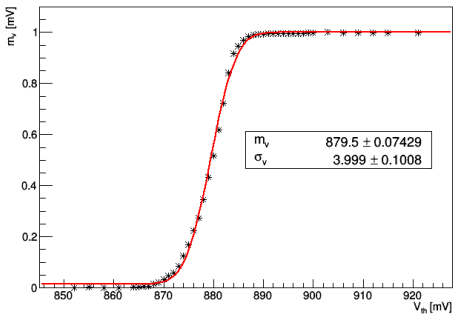

Figure 6: S-curve to calculate front-end noise (in mV, corresponding to $800\,e^-$ ENC)

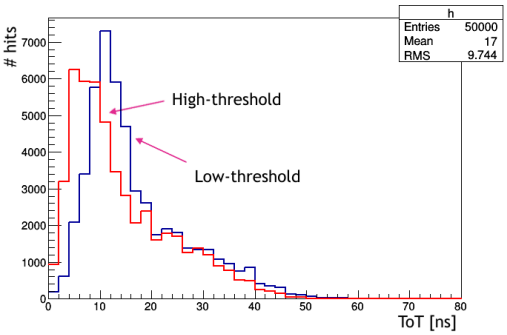

Figure 7: Peaks for a ^{90}Sr source (blue: low threshold, red: high threshold)

The chip was found to be fully working, both with standard and high-resistivity (1 kΩ cm) substrates. Figure 6 shows an S-curve used to calculate noise of the Front-end. The higher result compared to simulation can be explained with a higher input capacitance than expected, due to the presence of longer routing lines and pad compared to a fully monolithic structure. These effects will of course be much reduced in the final design, where pixels will be integrated on the same substrate as the electronics. Tests performed with an external 100 µm thick silicon sensor showed that the circuit was clearly able to distinguish particles from a ^{90}Sr source (see figure 7). Measurements with a test beam to assess the chip timing performance are currently in progress.

5. Conclusions

The main concepts of the design of the monolithic ASIC for the TT-PET project were shortly summarized here, along with the description of the scanner currently in development. The chip features a novel SiGe BiCMOS Front-end designed specifically for low-jitter timing measurements, integrating the sensor on the same substrate as the electronics. Simulations show the possibility of reaching a ~30 ps time resolution for 511 keV photons, using 135 µW per channel on 500 µm by 500 µm pixels. First test results on a prototype show good results, while more tests are being performed at the time of writing.

References

[1] TT-PET project, SNSF grant CRSII2-160808

[2] S. Vandenberghe and E. Mikhaylova and E. D'Hoe and P. Mollet J. S. and Karp, *Recent developments in time-of-flight PET*, *EJNMMI Physics, vol 3, issue 1, 2016*

[3] E. Ripiccini on behalf of the TT-PET collaboration, *The TT-PET project: A thin TOF-PET scanner based on fast silicon detector technology*, presented at *PSMR 2017*, publication pending

[4] L. Paolozzi, *Development of particle detectors and related Front End electronics for sub-nanosecond time measurement in high radiation environment*, *PhD thesis at University of Roma Tor Vergata, 2014*

[5] M. Benoit et al., *100 ps time resolution with thin silicon pixel detectors and a SiGe HBT amplifier*, *Journal of Instrumentation, vol 11, issue 3, 2016*