PROCEEDINGS OF SCIENCE

Electrical and functional characterisation with single chips and module prototypes of the 1.2 Gb/s serial data link of the monolithic active pixel sensor for the upgrade of the ALICE inner tracking system

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The upgrade of the ALICE Inner Tracking System uses a newly developed monolithic active pixel sensor (ALPIDE) which will populate seven tracking layers surrounding the interaction point. Chips communicate with the readout electronics using a 1.2 Gb/s data link and a 40 Mb/s bidirectional control link. Event data are transmitted to the readout electronics over microstrips on a Flexible Printed Circuit and a 6 m long twinaxial cable.

This paper outlines the characterisation effort for assessing the Data Transmission Unit performance of single sensors and prototypes of the detector modules. It describes the different prototypes used, the test system and procedures, and results of laboratory and irradiation tests.

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1. Introduction

The ALICE experiment at the CERN Large Hadron Collider studies strongly interacting hadronic matter by using nucleus-nucleus, proton-nucleus and proton-proton collisions. The next long shutdown period (2019–2020) foresees an upgrade of the Inner Tracking System (ITS) [1]. The new ITS will use about 25000 ALPIDE chips: custom large area CMOS Monolithic Active Pixel Sensors (MAPS) [2]. They are arranged in seven cylindrical layers surrounding the interaction point. Each layer is segmented into staves.

In the three innermost layers, a stave contains nine sensors. Each sensor sends data directly to the readout electronics over a dedicated data link. In the four outer layers each stave is segmented into half-staves and modules. One half-stave is built out of four (middle layer) or seven (outer layer) modules. One module combines 14 sensors in a master/slave configuration, with two master chips controlling six slave chips each. Every master chip has a data link to the readout electronics. Slave data are forwarded on a local bus to the master chip. The operating bit rate for the data links is 1.2 Gb/s for the three inner layers and 400 Mb/s for the four outer layers. The sensor differential driver strength can be adjusted in 16 steps from 0 to 5 mA for the main driver, and 0 to 2.5 mA for pre-emphasis [3]. The physical medium includes aluminium (inner layers) or copper microstrip traces on the Flexible Printed Circuits (FPC) and a 6 m long twin, mini-coaxial cable to the readout electronics.

This paper outlines the characterisation effort for assessing the Data Transmission Unit (DTU) performance of single sensors and prototypes of the detector modules: Section 2 describes the different prototypes used and Section 3 the test system and procedures. Results of laboratory and irradiation tests are presented in Section 4.

2. Sensor, module, and stave prototypes

Different prototypes for single chips and modules were used for sensor tests and characterisation. Single chips were mounted on carrier boards (Fig. 1), which provide connection for powering and signal transmission as well as probing points for the chip signals.

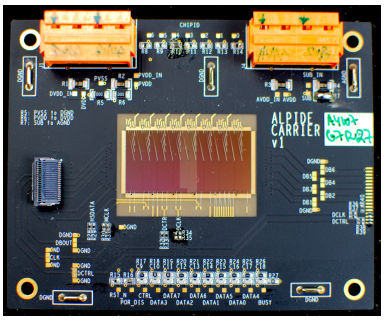


Figure 1: Single sensor carrier board

We used inner layer stave prototypes which had nine sensors installed on an FPC. Power was provided by a power network emulation board. Outer barrel staves were tested with two separate setups. For single modules, an outer barrel module prototype (Fig. 2) was used, populated with 14 sensors (two masters). It was powered over cross cables (in emulation of the final power distribution topology) and a power network emulation board. The module was used to test the communication between master chip and slave chips as well as the signal integrity while the sensors were active. An outer barrel half-stave prototype was used for full stave characterisation, consisting of single chip carriers connected via unpopulated FPCs. This emulated the signal transmission over the microstrip lines of the half-stave and the mini-coax cable to the readout electronics.

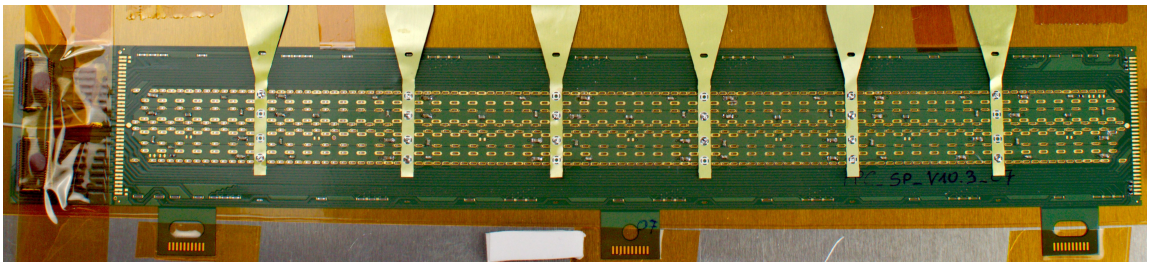


Figure 2: outer barrel module with 14 sensors (two master chips with six slaves each).

3. Test system and procedures

We characterised all sensors and modules using prototypes of the final readout system (readout electronics [4], cables, connectors). The firmware on the readout board communicated with the sensor over a control link. The data links were connected to the FPGA's serial transceivers. The readout board was controlled by a host computer over USB. A set of Python scripts provided a configuration interface to the FPGA's firmware modules. The interactive Python framework *Jupyter* was used for the rapid prototyping of test routines and the implementation of hardware features. Final test procedures were integrated in automatised test scripts to increase repeatability and ease of use.

The implemented test routines covered functional and signal integrity tests of the sensor control and data links. Functional tests included continuous communication over the control link and data transmission from the sensor. Either fixed event data or a pseudorandom binary sequence (PRBS)-7 signal were transmitted for data integrity checks. The firmware included a PRBS checker and event protocol checker to verify correct data transmission. Electrical signal integrity measurements were performed by recording statistical eye measurements on the receiving channel. This used features of the FPGA's serial transceivers to sample a signal with a horizontal and vertical offset and then compare it to a central sample point. By measuring the bit error rate (BER) at different offsets, we recorded eye diagrams (2D) and bathtub diagrams (phase offset).

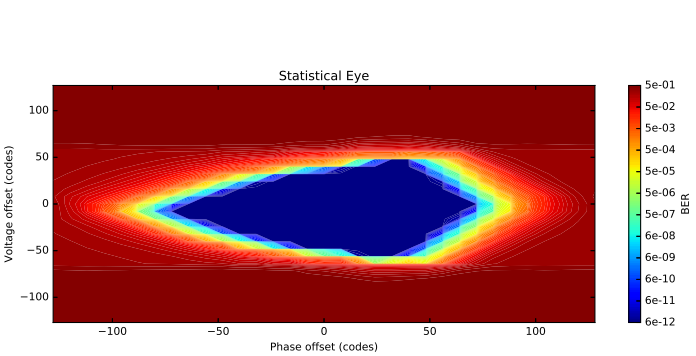
3.1 Beam tests

Single-chip carriers were irradiated with a 30 MeV proton beam at the Czech Academy of Sciences in Řež [5], with a particle flux ranging from 10^7 to 4×10^8 cm^{-1} s^{-2}. Three sensors were tested, accumulating a total ionising dose (TID) of 214, 346 and 470 krad, respectively. The same test setup as for laboratory characterisation was used. Reliability of both control communication and data transmission were tested over the range of supply voltages and data rates. The readout board was checking for radiation induced data upsets in the sensor data transmission unit by receiving and checking PRBS signals or event streams. In parallel, the signal quality of the data line was measured, using the recording of bathtub data. Having both signal quality and data measurements, the cause of an error could be linked to either single event upsets or a degradation of signal quality.

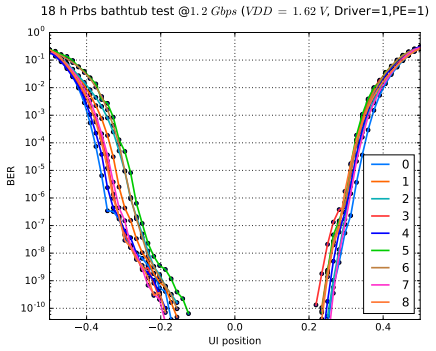
4. Test results

Testing results of the laboratory characterisation and irradiation campaign confirm a reliable

operation of the serial data communication. Stable communication is achieved over the full range of settings and operating conditions. Statistical eye diagram measurements show a horizontal eye opening of 0.5 UI and a 30% opening of its vertical range at a BER of 6×10^{-12} for *minimum* settings of the line driver (Fig. 3a). The measured RMS jitter is 27 ± 7 ps, depending on operating voltage and sensor matrix activity. A total of 109 h of accumulated signal integrity measurements on single chip modules show an upper limit for the BER of the transmission line of $\leq 9.8 \times 10^{-15}$ with a confidence level (CL) of 99%.



(a) Statistical eye of a single link with minimum driver settings of the DTU.



(b) Bathtub plot of an inner barrel module with nine chips

Figure 3: Statistical eye and bathtub plots captured by the transceiver margin analysis functionality of the FPGA

For inner barrel module prototypes, the measured BER was $\leq 7.9 \times 10^{-16}$ (CL 99%, $>$ 250 h of data). Supply voltage and sensor matrix activity have shown to have an influence on the horizontal opening of the statistical eye. Measurements taken at corner conditions (lowest supply voltage, minimum driver strength, expected sensor matrix activity) showed a horizontal eye opening of 0.3 UI at a BER of 5×10^{-11} (Fig. 3b).

Electrical measurements of the outer barrel half-stave transmission line showed a vertical eye opening of 340 mV measured at the input of the readout electronics. Increasing the length of the mini-coax cables to 8 m decreased the eye opening to 185 mV, which is within the requirements of the receiver. Measurements were taken at 400 Mb/s and mid range driver settings. PRBS measurements taken at 600 Mb/s gave an upper limit of the BER of $\leq 4.2 \times 10^{-15}$(CL 99%). Cross-talk tests showed no decrease of signal quality due to multiple chips sending data in parallel. Functional communication tests of outer barrel modules showed that stable communication was achieved for master-slave chip communication. No communication error between master and slave chips were observed.

Single-chip carriers have been tested in radiation for an equivalent of more than 1000 h of operation for a sensor in the innermost layer (the three layers of the inner barrel consist of 108, 144 and 180 sensors). During the radiation tests, we did not observe any errors in the data stream or control communication. The measured signal integrity showed no effect of radiation or single event effects on the data transmission unit's analogue components. Jitter measurements on post-irradiated chips showed no signal degradation after irradiation.

5. Conclusion

In this paper we present the techniques and experimental results of the characterisation of the Data Transmission Unit of the ALPIDE pixel sensor. The implemented framework for testing the chip has proven to be an efficient and flexible structure for both rapid test development and automated procedures.

The gathered results show that a stable data transmission is achieved under the expected radiation conditions. The electrical margins are within the requirements, and there was no indication of malfunctioning of the Data Transmission Unit due to radiation effects.

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