

# Functional Tests of 2S Modules for the CMS Phase-2 Tracker Upgrade with a MicroTCA-based Readout System

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First full size 2S module prototypes for the CMS Phase-2 Outer Tracker Upgrade have been assembled. With two sensors of realistic dimensions and 16 CBC2 readout ASICs on two front-end hybrids, the characteristics of these novel and complex objects can be studied.

A MicroTCA based readout system was developed to test multiple front-end hybrids simultaneously. Therefore the concurrent information of the full module can be used for noise and signal studies.

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## 1. Overview

To prepare the CMS experiment for the High Luminosity LHC [1] era and its planned instantaneous luminosity of up to  $5 - 7.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$  the CMS Silicon Tracker is planned to be replaced in the Long Shutdown 3 (LS3) around the year 2024 [2].

The original Silicon Strip Tracker was designed for a total fluence equivalent to an integrated luminosity of about  $600 \text{fb}^{-1}$  [3]. It is expected that after about  $1000 \text{fb}^{-1}$  the silicon sensors of the Tracker will enter *thermal runaway* - a situation where the cooling capabilities of the modules are surpassed by power dissipated in the sensors, caused by the increase of the leakage current. Therefore it is required to replace the current Tracker before the LHC starts with the High Luminosity operation after LS3 and is expected to deliver a yearly integrated luminosity of about  $300 \text{fb}^{-1}$ .

To reach this goal, up to 200 proton-proton collisions per bunch crossing (pileup) are required, surpassing the current value by a factor of about 5 and the original LHC design by about 10. CMS plans to introduce tracking information into the first trigger stage in order to keep the same sensitivity as today. It is foreseen to reconstruct all tracks having a transversal momentum ( $p_T$ ) above a threshold of about 2 GeV within  $4 \mu\text{s}$  as part of the first trigger stage in CMS.

Since the bandwidth between the silicon strip modules and the counting room is constrained by the material budget in the active tracking volume, the transversal momentum threshold is applied within the front-end ASICs on the modules. This filter exploits the 3.8 T solenoidal magnetic field of CMS - which forces charged particles on a circular motion with respect to the transversal collision plane of the event. Therefore hits of a charged particle in two silicon strip sensors placed in a distance of 2 – 4 mm to each other are already displaced significantly. Since the displacement is inverse proportional to the  $p_T$ , a maximal displacement of the two hits can be related to a minimal threshold for the track  $p_T$ .

The design of all Outer Tracker modules is driven by this principle. Each module hosts two stacked silicon strip sensors and common front-end electronics, allowing to search for correlated hits in both sensors [2]. Two module types are foreseen: 7680 so-called 2S modules with two identical  $\sim 90 \text{cm}^2$  sized strip sensors are required to cover the large area of the outer layers (60 – 120 cm), while 5616 PS modules with smaller and more segmented sensors ( $\sim 45 \text{cm}^2$ ) provide higher granularity and enhanced resolution for the inner layers (20 – 60 cm).

## 2. 2S Modules

Each sensor of a 2S module is segmented into two rows of 1016 strips with a pitch of  $90 \mu\text{m}$  and a length of 5 cm, resulting in an active sensor area of  $90 \text{cm}^2$  per sensor (Fig. 1). Two sensors are glued to spacers (with a height tuned for an optimum working point for the  $p_T$  discrimination depending on the module position) and providing the mechanical mounting points. On two sides the front-end hybrids (FEH) are placed next to the sensor to connect one row of strips of each sensor to the same FEH. Then 127 channels from each sensor are connected to a common readout ASIC - the CMS Binary Chip (CBC) [4] - resulting in 8 CBCs per FEH. Consequently each CBC has access to the hit information of both sensors and is able to correlate hits utilizing relatively simple logic after discriminating the analogue pulses with a single common threshold to a binary hit signal per strip.

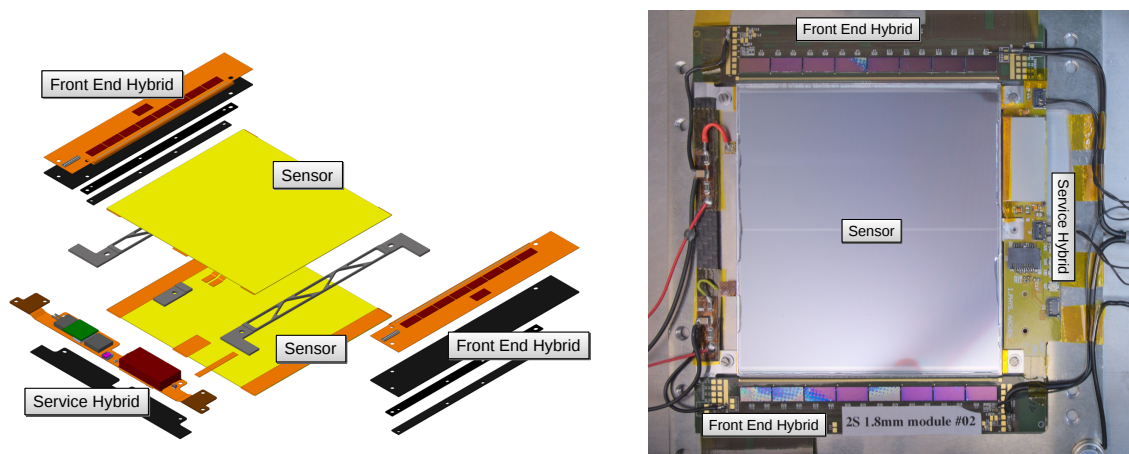


Figure 1: Left: Exploded view of the 2S module [2]. Right: Photo of a full-size 2S module prototype equipped with a service hybrid.

Auxiliary electronics and the connection points for all services are hosted on the service hybrid (SEH) which is mounted on one of the sensor edges that is not occupied by a FEH and connected to both FEHs. The Low Power Gigabit Transceiver ASIC [5] merges the data streams of both FEHs into a single 4.8 Gb/s upstream, while it also provides slow control and clock and commands for the FEHs via a 2.56 Gb/s downstream. The Versatile Link PLUS [6] package is bridging the electrical and optical domains of this high speed data link. All ASICs are powered with a point of load concatenated DC-DC-DC conversion scheme, providing 2.55 V for some of the optoelectronic components and 1.2 V to all other ASICs, while a source voltage of 12 V is provided to each module individually throughout the Outer Tracker.

### 3. Module Prototypes and Readout System

Current 2S module prototypes (Fig. 1) feature close to final sensor geometry and layout resulting in a realistic strip capacity ( $\sim 9$  pF), one of the leading influences on noise in analogue front-ends. The two FEHs host the second not final version of the CBC ASIC, which is realistic in aspects of analogue performance but does not yet feature the final data output format and signal types. Therefore the CBCs are controlled and read out using a level translator and adapter card and high density LVDS cables to connect to the CERN Gigabit Link Interface Board (GLIB) [7].

The original readout system was expanded to read out both front-end hybrids of one module simultaneously with two GLIBs. Both are using a common 40 MHz clock which is distributed via the backplane of a commercial MicroTCA [8] crate. Enable and trigger signals are also shared between both GLIBs via a 40 MHz clocked M-LVDS bus.

The communication between the custom developed firmware and the readout computer is realized with the IPbus-protocol [9] over a 1000BASE-T Ethernet connection. Achievable readout speeds reach 10000 events per second and are sufficient for functional tests on the bench in the laboratory.

## 4. Measurements

One of the main measurement objectives with the full size module prototypes was the characterization of the noise present in the analogue front-end of the readout ASIC when operated under realistic conditions, especially in terms of input capacitance (sensor dimensions) and power provision. Therefore one module was equipped with a service hybrid prototype and modified to allow a switch-over between direct powering with a conventional power supply and the use of the DC-DC converters on the SEH (Fig. 1).

The noise present in each channel of each CBC is determined with a threshold scan near the 50% occupancy<sup>1</sup> point,  $\mu$ . In absence of any signal from charged particles in the sensor, at this point the net input charge into the analogue front-end is zero. Statistical fluctuations in the analogue front-end output voltage (and the comparator threshold) caused by internal and external influences are collectively called *noise* (denoted  $\sigma$ ) and can be extracted by a fit of a cumulative distribution function to the obtained occupancy values as a function of the set threshold,  $\tau$  (Fig. 2):

$$\text{Occupancy}(\tau) = \frac{1}{\sigma\sqrt{2\pi}} \int_{\tau}^{\infty} \exp\left(-\frac{1}{2}\left(\frac{\mu-x}{\sigma}\right)^2\right) dx$$

To relate the obtained noise to a potential signal induced by a charged particle, the comparator threshold DAC voltage and subsequently the noise is expressed in charge equivalent to a signal pulse injected into the front-end using internal test-pulse capacitors.

The measured noise for each channel of the module's 16 CBCs corresponds to 800 to 1000  $e^-$  depending on the CBC position (Fig. 3). These values are comparable to earlier measurements on smaller module prototypes with two CBC2s with similar strip geometries and have been achieved with the foreseen analogue power budget of 0.35 mW per channel. Dependencies on sensor bias

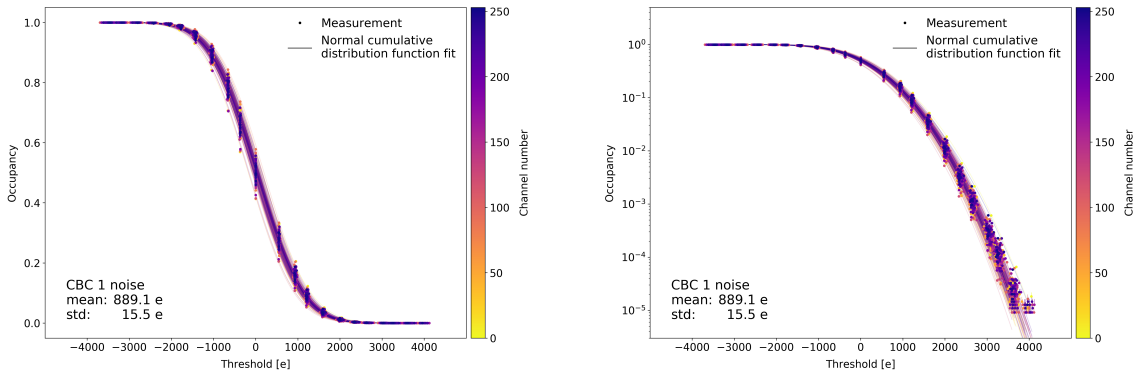


Figure 2: Noise measurement for a single CBC2. Occupancy is measured as a function of the comparator threshold. The noise is extracted as the width of the cumulative normal function fit. For this measurement the module was operated in a low humidity environment at a stable temperature of  $+16^{\circ}\text{C}$  and a bias voltage of  $-300\text{ V}$  applied to the sensor.

<sup>1</sup>Fraction of events for which the analogue front-end output voltage exceeds the comparator voltage at the time of triggering.

voltage have been found to be negligible, once full depletion (of these unirradiated sensors) has been achieved. An average trigger frequency of 100 kHz, close to the maximum trigger rate of the CBC2 (limited by data output speed) was used.

When comparing the noise in channels of the upper sensor closest to the sensor edge (CBC 15) in the measurement with and without the use of a DC-DC converter, a slight increase towards the sensor edge, at which the DC-DC converters are situated on the FEH (distance to sensor < 1 mm), becomes apparent. It is plausible that the high frequency electromagnetic emissions caused by the duty cycle of the DC-DC converters are responsible for this local increase in noise, since the effect decreases very fast with distance. The current SEH encases all active components of the converters (ASICs, main inductors and filter components) with a 150  $\mu\text{m}$  thick Aluminium box, which is placed on the SEH and soldered to its reference ground plane. While the effect could be decreased with an additional layer of 60  $\mu\text{m}$  of copper foil on the shield face towards the sensor, the exact origin and frequency composition of the coupling mechanism is under investigation and will have influence on the next iteration of the SEH.

Even if no further improvement in this area can be achieved, only a very limited number of channels (< 30) out of 4064 per module would fail the specification of a maximum noise of 1000  $e^-$ , therefore currently this is not a point of concern. Projections foresee seed strip signals of 12000  $e^-$  when subjecting the silicon sensor to a fluence equivalent to twice the full program of the HL-LHC. In combination with the fact that even at low occupancies (<  $10^{-3}$ ) no deviation from a normal distributed noise was observed (Fig. 2), this provides enough headroom for a good signal to noise discrimination even at the end of the lifetime of the 2S modules.

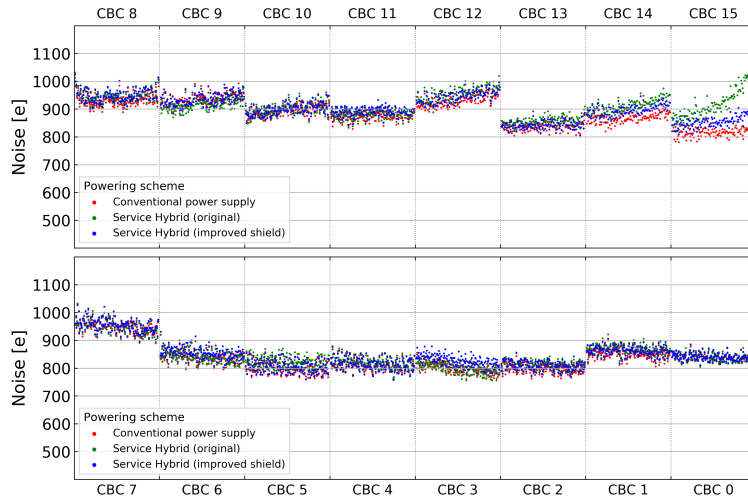


Figure 3: Noise measurement of different powering scenarios for all channels of one 2S module prototype. The upper right CBC 15 is situated closest to the DC-DC converter on the service hybrid. For CBC 13 – 15 only the upper sensor channels are shown, since the lower sensor has been accidentally disconnected in this region.

## 5. Summary

For the CMS Phase-2 Outer Tracker Upgrade all modules will feature two stacked silicon strip sensors and conceptually new front-end ASICs, which allow to discriminate hits from tracks of charged particles by their  $p_T$ . All hits of tracks above a  $p_T$  threshold of about 2 GeV are streamed to the Track Trigger component of the first trigger level and provide an important handle to fully exploit the unprecedented event rates the High Luminosity LHC will provide after LS3.

Current designs foresee for the outer layers of the tracker the use of 7680 2S modules, of which first full size prototypes have been assembled. Functional tests were carried out, focusing on the characterization of the noise in conjunction with a realistic powering scenario. When comparing measurements utilizing a service hybrid prototype and the incorporated DC-DC converters with a conventionally powered scenario for more than 95 % of all 4064 channels no difference in noise can be observed. More than 99 % of all channels meet the specification of a noise  $< 1000 e^-$  in these tests.

Both front-end hybrids and service hybrids of the 2S modules are expected to become available within the upcoming months in improved and closer to final revisions, including the latest versions of the essential ASICs and well defined interfaces. This provides the possibility to evaluate the full module and all of its foreseen features in a single assembly and allows to gain a deeper understanding of the interplay between individual components of these complex objects.

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