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ATLAS ITk Short-Strip Stave Prototypes with 130 nm chipset

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The ATLAS ITk Collaboration is working to deliver a new Inner Tracking detector for use at HL-LHC. The strip tracker community has recently constructed a partially loaded, double-sided demonstrator stave using the HCC / ABC130 chipset in 130 nm CMOS technology. Mindful of the need to maximise power efficiency whilst minimising the cost and material of associated cable plant, the system design includes the integration of a low-mass DC-DC converter and sensor bias (HV) switch within each module. This paper documents the first results from the demonstrator stave. The system concept is also outlined.

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1. Introduction

The ATLAS ITk Collaboration is working to deliver a new Inner Tracking detector for use at HL-LHC. As detailed in the Technical Design Report [1], the strip tracker applies a common system architecture to two geometrically different regions: four concentric barrels composed of staves, and two endcaps comprising disks which are further segmented into petals.

Each stave or petal comprises a support structure made of carbon fibre and foam into which a cooling pipe has been integrated. Polyimide flex circuits known as “bus tapes” are co-cured upon them to route electrical services between the End of Substructure (EoS) card, which provides the interface to the off-detector systems, and the detector modules which are glued to the surface of the bus tape. This year our community has constructed a partially loaded, double-sided demonstrator stave using the HCC / ABC130 chipset in 130 nm CMOS technology, for which results are reported here. The system architecture of this stave differs slightly from that proposed for production units with the ABCStar / HCCStar chipset in the same technology, but is sufficiently representative so as to make this an important test.

2. Architecture of the On-Detector Electronics

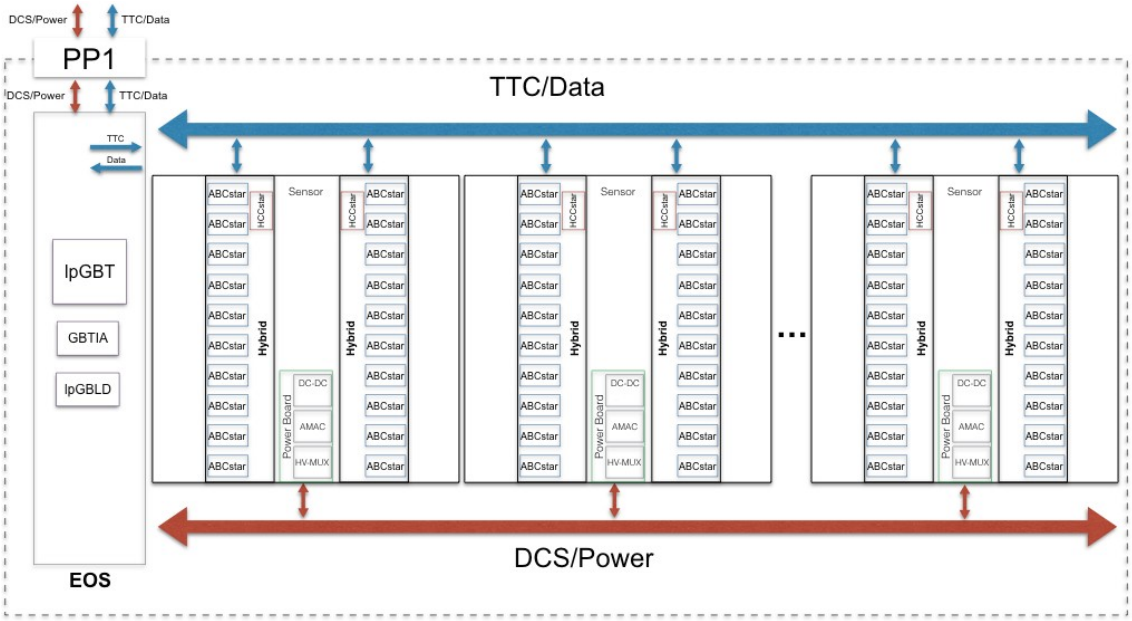

Figure 1: Architecture of the ITk Strip On-Detector Electronics (from ATLAS-TDR-025).

The architecture of the ITk Strip On-Detector Electronics is shown in Figure 1. At the left-hand side of the image, the End-of-Substructure (EoS) card [2] links the off-detector systems, both electrical and optical, to the petal or stave. Petal and stave layouts will differ, but the concept and schematics will be largely common. The board will use the lpGBT chipset [3] to convert Timing, Trigger and Control (TTC) information, received in optical form by means of Versatile Links PLUS (VL+) [4], into the Scalable Low-Voltage differential signalling (SLVS) signals needed by the front-end ASICs. These will route along one edge of the petal or stave’s bus tape (shown in blue). The TTC information is transmitted on a series of multidrop buses,

four per stave side, each comprising three SLVS differential signals and serving up to 10 hybrids at 160 Mbit/s. Each hybrid returns point-to-point event data to lpGBT at 640 Mbit/s.

In order to maximise power efficiency and to minimise the cost and material of associated cable plant, each stave or petal side has a common low-voltage power bus at 11 V. Low-mass DC-DC converters on the strip modules and indeed the EoS board are used to deliver the lower voltages needed to power the Application Specific Integrated Circuits (ASICs), 1.5 V in the case of the front-end chipset. Similarly the number of high-voltage buses used to provide sensor bias to the fourteen modules of each stave side at up to 700 V is reduced to four: on-module HV switches are used to disconnect any failing sensors from the bus. These low- and high-voltage buses route along the other edge of the bus tape together with the Power Board control signals.

The module design and standalone performance were detailed elsewhere in this conference [5]. Two Polyimide Flex Hybrids are glued onto a Silicon Strip sensor which is approximately 97 mm by 97 mm. The sensor has four banks of 1280 strips, 75.5 μm pitch, each bank being 24.1 mm long. Each hybrid has one Hybrid Controller Chip (HCCStar) and ten ATLAS Binary front-end Chips (ABCStar), so named because point-to-point links send data from each front-end chip back to the HCCStar chip in a star topology. The ABCStar has a binary architecture with 256 trimmable preamplifier / discriminator channels, pipeline and control logic. Dual integrated Low DropOut (LDO) regulators produce separate 1.2 V analogue and digital power domains from a common 1.5 V supply.

Also glued to the sensor, between the hybrids, is the Power Board. This integrates a Point-of-Load (PoL) DC-DC converter using the bPOL12V ASIC, based upon the FEAST2 chip [6]; a high voltage switch “HV-MUX” based upon a radiation hard GaNFET [7]; the Autonomous Monitor And Control (AMAC) chip with logic to turn on or off low-voltage and/or high-voltage power to hybrids or sensors in response to commands or anomalous readings from its integrated, multichannel Wilkinson ADC; and linPOL12V, a dual linear regulator based upon IP from bPOL12V, which powers AMAC independent of the DC-DC converter. AMAC measures the sensor bias return current by means of an operational amplifier, in addition to temperatures, low voltages and power currents.

3. First Short-Strip Stave Prototype

There are several differences between the architecture of the first Short-Strip stave prototype and the architecture of the final system. The stave is only 13 modules long instead of 14 and uses a single, non-segmented TTC bus to serve all hybrid locations. As a result of previous tests of signal integrity on this bus tape design [8], the population of the stave was restricted to four modules on each side, akin to one TTC segment of the final design. The bus tape has only two HV lines per side instead of the planned four and, for purposes of readout, uses a fully electrical End-of-Substructure card coupled to a commercial FPGA board by ribbon cables. An SLVS buffer was also added to shift the common-mode level of the (previously) Low-Voltage Differential Signalling (LVDS) TTC signals and boost their amplitude twofold.

The modules of this stave use the earlier HCC/ABC130 chipset which routes event data according to a “loop” topology: each hybrid has two loops of five ABC130 chips, with a data connection to HCC at each end of the loop. Power boards with AMAC were not yet available hence commercial components were used to provide the oscillator from which the GaNFET gate voltage is derived (by means of a capacitively coupled voltage multiplier), and to turn the

oscillator and DC-DC (using the FEAST2 chip) on and off. Local monitoring is provided by the Autonomous Monitor within HCC which reads voltages, temperatures and the sensor return current; IP which was later developed into the AMAC chip. The HV-MUX circuitry is only fitted to the modules on one side of the stave, which is the side shown in Figure 2.

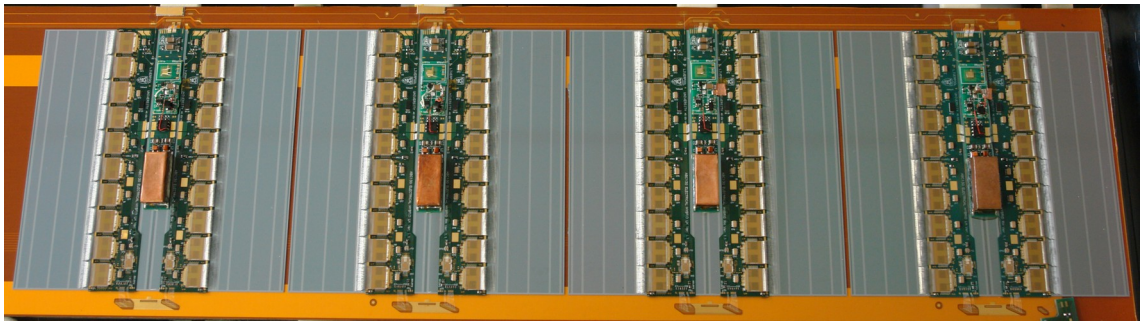

Figure 2: Photograph of one side of the Short-Strip stave prototype.

4. Results

The oscillator used to drive the power board's voltage multiplier (and hence the GaNFET) was found to be a source of excess occupancy as shown in Figure 3, but this was corrected by the addition of a local RC filter to transform its output from a square to sawtooth waveform. A comparison of noise values obtained for the modules on-stave and off-stave is shown in Figure 4. For a series of injected charges, threshold scans are recorded and fitted to determine the correspondence between charge and threshold, and hence the gain. The width of the s-curve recorded for 1fC injected charge is divided by the gain to determine the input noise in fC. In the figure each dot represents the mean input noise for one of the two banks of 128 strips served by the 256-channel chip. The noise is approximately 15 electrons higher on-stave than off-stave, but the correlations between the two sets of results are strong. The stave now performs very well: no difference in performance between the two sides has been observed and results are stable across several days. The expected relationships between the measured noise and sensor bias voltage, and between the measured noise and the number of pulsed channels, have been observed. An "aggressor" test, in which an additional short-strip module was placed under the stave to approximate the effect of overlapping staves in the experiment, has shown no ill effects. A preliminary test to operate the stave from a second external DC-DC stage, one of the options under consideration for the off-detector power distribution, was also successful.

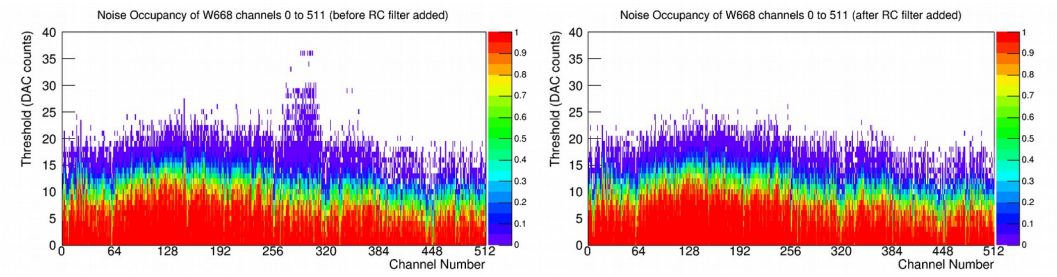

Figure 3: Excess occupancy correlated with the HV-MUX circuitry (left) was resolved by the addition of an RC filter (right). The plots show raw pedestal scan data, initially with extra hits at high thresholds for affected channels. The motivation was the identification and elimination of external noise sources: the equivalent noise charge was not determined at this stage.

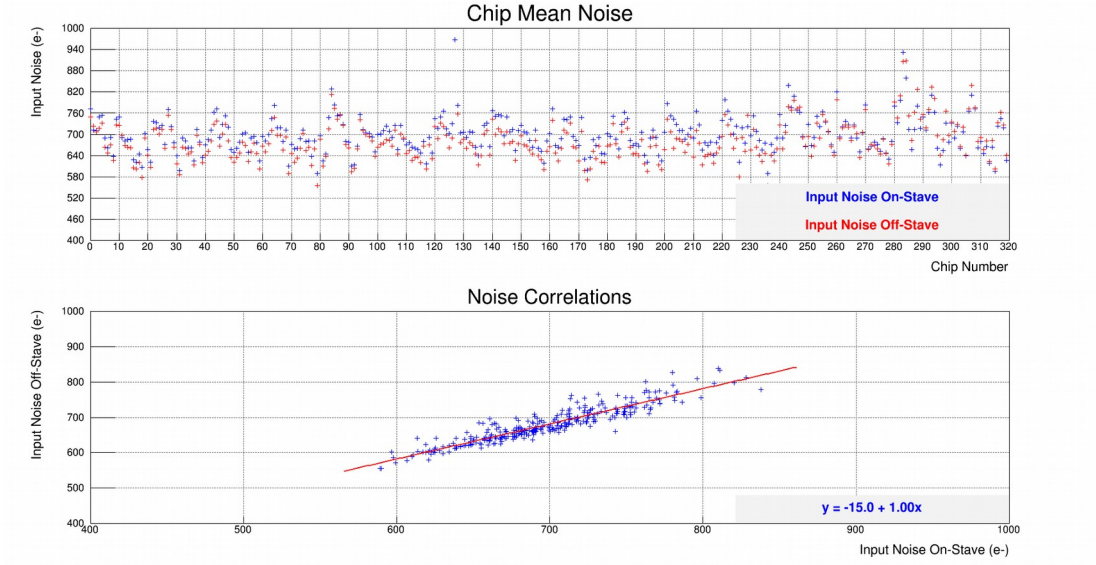

Figure 4: Input Noise (Equivalent Noise Charge) for the modules on- and off-stave.

5. Conclusion

This important study has verified that certain novel aspects of our chosen module and stave designs have no ill-effects in terms of noise: the use of power boards hosting miniature DC-DC Buck converters glued directly to the sensor surface; the oscillator-driven high-voltage switch located on-module ("HV-MUX"); the addition of sensor bias return current monitoring in the Hybrid Controller Chip (HCC); the use of a common on-stave return bus for both low-voltage and high-voltage (sensor bias) currents. The aggressor test is also an important result, showing that the DC-DC converters of opposing staves do not interfere with their neighbours.

References

[1] ATLAS Collaboration, *Technical Design Report for the ATLAS Inner Tracker Strip Detector*, ATLAS-TDR-025.

[2] P. Goettlicher et al., *The End-Of-Substructure Card for the ATLAS ITk Strip Tracker*, Proceedings of this conference (2017).

[3] https://espace.cern.ch/GBT-Project/LpGBT/Specifications/LpGbtxSpecifications.pdf

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[5] A. Greenall, *ATLAS ITk Short-Strip Stave Prototype module with Integrated DCDC Powering and Control*, Proceedings of this conference (2017).

[6] F. Faccio et al., FEAST2: A Radiation and Magnetic Field Tolerant Point-of-Load Buck DC/DC Converter, Proceedings of IEEE Radiation Effects Data Workshop, 10.1109/REDW.2014.7004569

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