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Studies on the Readout of the ATLAS Inner Tracker Using Commercial Networking Hardware

Carsten Duelsen*, **Tobias Flick, Wolfgang Wagner, Marius Wensing**
Bergische Universitaet Wuppertal
E-mail: carsten.dulsen@cern.ch

In the context of the ATLAS Phase-II upgrade, new front-end electronics is developed, which is read out with up to 5.12 Gb/s per link due to finer granularity and higher occupancy.
Because of the high bandwidth requirements, new concepts are needed for the ATLAS **I**nner **T**rac**k**er (ITk) readout system. A new scalable approach based on many rather simple nodes is proposed to support lab setups, testing sites as well as the readout of large detector parts. This study is focused on the use of COTS networking components to reduce the costs and increase the flexibility of such a system. Results from first studies are presented.

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*Speaker.

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1. Introduction

In the course of the HL-LHC upgrade (planned for 2024-2026) with expected luminosities of up to $5 \cdot 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ ATLAS will perform the Phase-II upgrade. During this upgrade the complete Inner Detector of ATLAS will be replaced by the new **I**nner **T**rac**k**er (ITk) [1].

Also the ATLAS trigger system will be upgraded for Phase-II. The current baseline is the full readout at L0 (1 MHz). The backup mode of operation is an increased L0 rate (up to 4 MHz are under discussion) and the readout at L1.

With a planned readout speed of 5.12 Gb/s per link, up to 4 links per module and around 10 000 modules, a combined data rate in the order of 100 Tb/s is expected. This amount of data needs to be taken care of within the fixed constrains (like space, power and money) given. Therefore, our proposed solution is based on rather simple nodes, being able to be packed into high density crates and using commercial networking parts. These nodes are also planned to be operated in standalone mode for production tests as well as laboratory or test-beam usage.

Finally, our solution follows the ATLAS TDAQ approach using FPGA cards as interface between the detector and the network (FELIX [2]). Therefore, our solution can provide a beneficial input for developing the final ITk readout system as critical topics (e.g. calibration) can be studied and development of firmware and software can be started.

2. Data Flow Scheme

The basic data flow scheme is shown in Figure 1. A local trigger interface provides access to the central trigger information (like trigger IDs) and forwards feedback signals (like busy) back to the central infrastructure. The calibration and run configuration are received via commercial networks. All these information are combined in the readout card, encoded in the frontend specific protocol and sent out to the detector.

The data coming back from the detector is received by the readout card through optical fibers and the custom protocol is decoded partially for a first error check. After this, the combined data

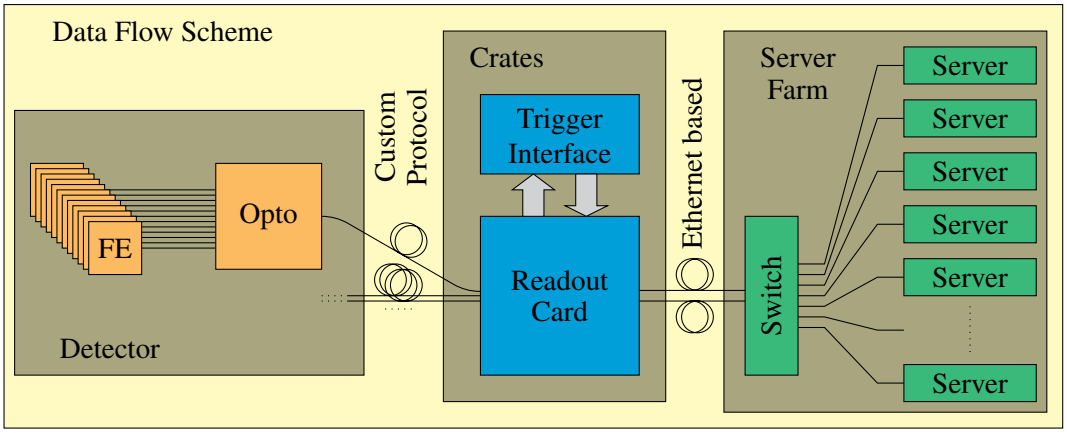


Figure 1: Data transmission scheme to be used in our proposed solution for the the ITk Pixel Detector.

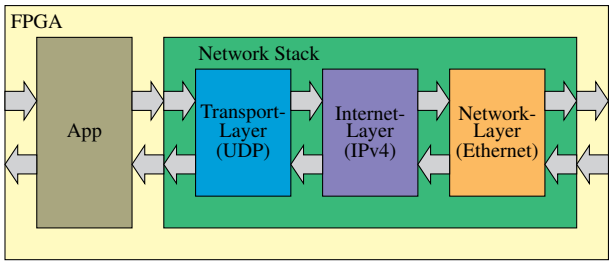


Figure 2: The building blocks of the network stack which is included in the readout card.

from different links is packed into packets and sent out using commercial networking protocols. To maximize the performance and reduce the number of needed parts at the same time, the network interface is realized within the FPGA on the readout card. For this first test implementation the network stack is running at 10 Gb/s and contains the following features:

- Ethernet, ARP, IPv4, ICMP (echo request/reply), UDP
- easy integration of additional protocols due to open interfaces (AXI Streaming [3])
- support for jumbo frames (limited only by IPv4 length field)

Support for 40 Gb/s operation is in development and a 100 Gb/s version is also planned.

3. Measurements

In Figure 3, the achieved payload bandwidth for different packet sizes is depicted. Data was sent in a UDP/IP stream with fixed package size from an FPGA board to another FPGA board (the purple line) and from the FPGA to a PC (green line). We also tried a Xilinx example design [4] using the ARM processor within the FPGA SoC as comparison (blue line).

In Figure 4, the measured packet loss rate for different packet sizes is shown. While no packet loss at all was encountered for FPGA board to another FPGA board and the ARM to PC tests, the

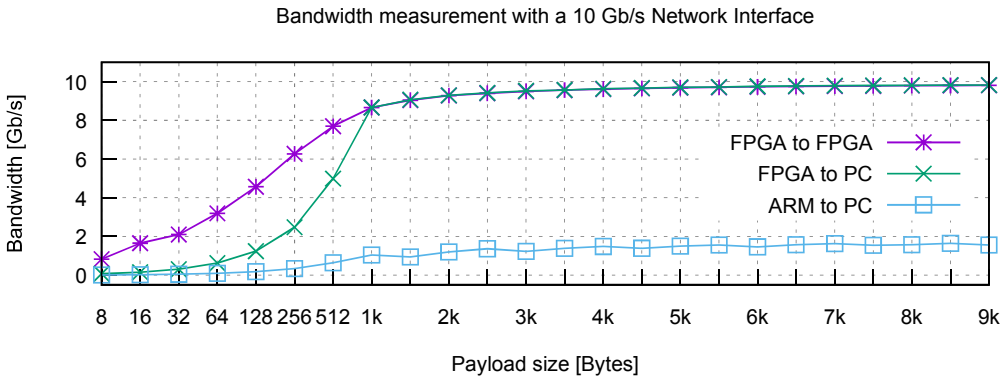


Figure 3: Results from bandwidth measurements for FPGA to FPGA, FPGA to PC and ARM to PC tests.

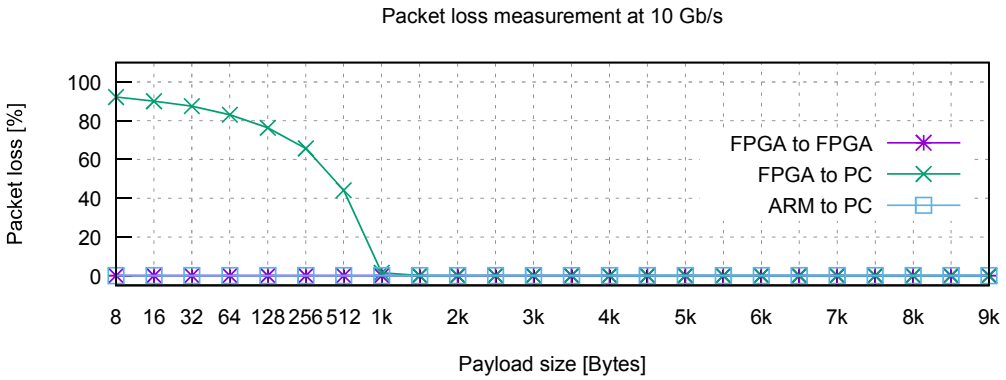
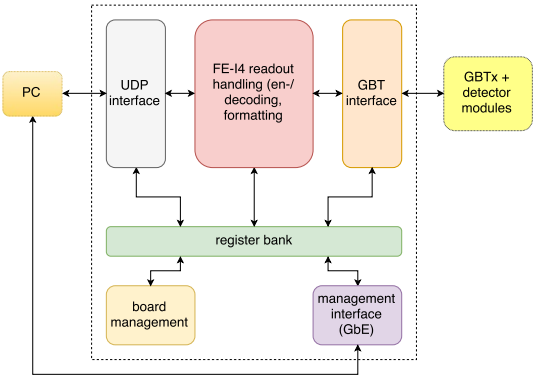


Figure 4: Results from packet loss measurements for FPGA to FPGA, FPGA to PC and ARM to PC tests.

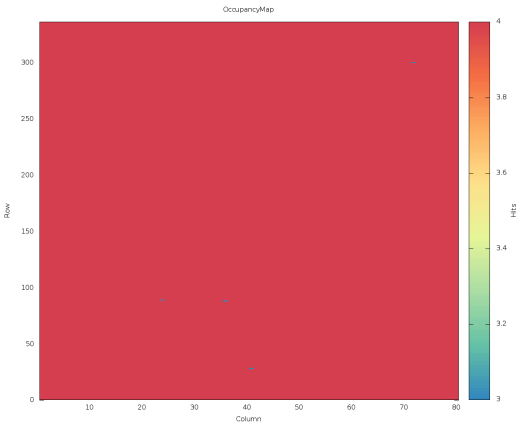
FPGA to PC tests show partly very high loss rates and never reached exactly 0. The behavior for small packets shows the maximum packet rate of around 1.2 million packets per second which can be processed by our test PC.

4. Application

An ITk demonstrator system test will be installed at CERN and will use old FE-I4-based [5] detector modules (total number of front-ends: 120) as the new modules aren't available yet. It uses a GBT ecosystem [6] as optical data link with 4.8 Gb/s data rate including a forward-error-correction and can be used to evaluate readout systems with high-speed optical data links. To make use of this opportunity, an "Off-Detector" readout system based on Avnet Kintex-Ultrascale



(a) Block diagram of the readout card firmware.



(b) Result of a digital injection scan with a single front-end chip. Gaps in the scan refer to lost packets.

Figure 5: Structure of the firmware and a scan result as prove that the whole chain is working.

Evaluation board [7] has been developed. The block diagram of the firmware is shown in Figure 5a. The central part is the front-end handling firmware plus supporting blocks for the GBT and UDP communication and currently supports one GBT link and one 10 Gb/s Ethernet link.

5. Conclusion

The new readout system was tested successfully and a first implementation is available. Calibration procedures can be executed through the high-level software. A digital injection scan with a single front-end chip is shown in Figure 5b to prove that the whole chain is working. The gaps in the scan refer to lost packets. Further integration of the readout system into the future ITk readout software framework is under preparation.

To be able to readout the complete system test, a scaled up version of the readout system with 8 GBT links (equal to 160 FE-I4s) and two 10 GbE interfaces is in development. Also, some work to improve the network reliability is required and the implementation of according protocols (e.g. RUDP, TCP, ..) will be explored in the near future.

Acknowledgments

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