

DRM2: the readout board for the ALICE TOF upgrade

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Abstract:

For the upgrade of the ALICE TOF electronics, we have designed a new version of the readout board, named DRM2, a card able to read the data coming from the TDC Readout Module boards via VME. A Microsemi Igloo2 FPGA acts as the VME master and interfaces the GBTx link for transmitting data and receiving triggers and a low-jitter clock. Compared to the old board, the DRM2 is able to cope with faster trigger rates and provides a larger data bandwidth towards the DAQ. The results of the measurements on the received clock jitter and data transmission performances in a full crate are given.

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1. Introduction

The ALICE Time Of Flight (TOF) detector [1] is a large array of 1593 Multi-gap Resistive-Plate Chamber (MRPC) strip detectors for particle identification in the intermediate momentum range at the ALICE experiment (CERN). Each of the 18 sectors is read out by four VME electronic crates, each hosting 9 or 10 TDC Readout Module (TRM) boards and one Data Readout Module (DRM) card. In order to cope with an increase of luminosity and of the interaction rate (up to 1 MHz in proton-proton collisions and 50 kHz in lead-lead collisions), we have designed a newer board, named Digital Readout Module 2 (DRM2). The card features a faster link towards the data acquisition system using the GBTx ASIC [2] and VTRx optical transceiver [3] from CERN, which allow to reach an user bandwidth towards the Data AcQuisition system (DAQ) of 3.2 Gb/s. The readout will be implemented with synchronous triggers at fixed bunch crossing values at 33 KHz, setting a matching window of 30 microseconds in the TDC ASIC installed in the TRMs, named the HPTDC. This solution will mimic a full-fledged continuous readout as all ALICE detector upgraded readout chains. The same link is also used for receiving triggers and a low-jitter clock, which is distributed to the front-end electronics. For the TOF detector the quality of this clock is crucial and a campaign of measurements on the clock received from the ALICE data acquisition card named CRU (Common Readout Unit) [4] has been carried out: we measured a RMS clock jitter as low as $O(10)$ ps, which is compatible with the requirements.

The paper presents the design details of the DRM2 board, together with the measurement results of the performances obtained working with DAQ cards (CRU and C-RORC), for what concerns the received clock quality and the data transmission bandwidth towards the DAQ.

2 DRM2 architecture

Fig. 1 shows a picture of the DRM2 board. It is a narrow 9U VME card (16 cm x 33 cm) with the same form factor as the DRM1 and the TRM boards. The heart of the board is a Microsemi Flash-based Igloo2 FPGA, which drives the trigger and data flows inside the crate. This device has been chosen since the expected TID (Total Ionizing Dose) for the board (placed 4 meters far from the beam pipe) is 0.13 krad in 10 years, which is acceptable for such a device. The advantage is that the FPGA configuration memory is SEU (Single Event Upset) immune, so that scrubbing is not needed [5].

The optical link towards the readout board (CRU) is implemented through the GBTx ASIC and the VTRx optical transceiver. These devices allow one to build a GBTx link with the following features:

- a high bandwidth data transmission towards the CRU (400 Mbytes/s);
- the same bandwidth in the opposite direction for receiving triggers and trigger information (80 bits per each 40 MHz clock cycle);
- the possibility for the DRM2 to receive a low-jitter clock from the CRU. The quality of the clock is of great importance for the TOF system, since it is used for high resolution timing measurements on the TRM boards on the HPTDC chips.

The FPGA – GBTx connection consists of a single 40-bit large parallel lane of 80 MHz differential signals. The same configuration was previously tested on a GBTx test board developed before designing the DRM2: we could measure a BER lower than 10^{-14} and a total jitter on the received clock around 50 ps [6].

The trigger / data flow inside the board can be described in the following way:

- a trigger is received through the GBTx link and passed to HPTDC via VME backplane;
- the DRM2 reads each TRM HPTDC data via VME and stores them in the on-board SSRAM device;
- when complete, the event is read out from the SSRAM and sent to the CRU via the GBTx link.

Since the plan is to run with a continuous trigger at 33 KHz, the sum of the time intervals required to fulfill all these operations should be lower than 30 μ s, so to avoid the assertion of the busy signal. For this reason we decided to increase the VME bandwidth for reading out the TRMs from 40 Mbytes/s (as it used to be on the DRM1) to 160 Mbytes/s, by implementing the 2eSST VME64x protocol. This allows the DRM2 (master of the VME bus) to readout the data from the TRMs (VME slaves) as 64 bit words on both rising and falling edges of the DTACK signal, which can be as fast as 10 MHz. This leads to a 160 Mbytes/s peak VME data throughput. Paragraph 3 shows the results of the performance measurements carried out in a full crate.

The DRM2 board features also two slow control links, which were also used on DRM1:

- A 1.28 Gb/s proprietary serial link (CONET2) from CAEN. This link is used for configuring the TRM boards, for reading temperatures and voltages and for monitoring physics data during data taking. The link is based on the Igloo2 internal high-speed SERDES;
- An Atmel ARM processor running Linux on a commercial piggy-back mezzanine (named A1500 from CAEN), whose purpose is to remotely re-program the Igloo2 FPGA via an Ethernet link when a new firmware revision is released. The same link is also used to implement other slow-control functionalities.

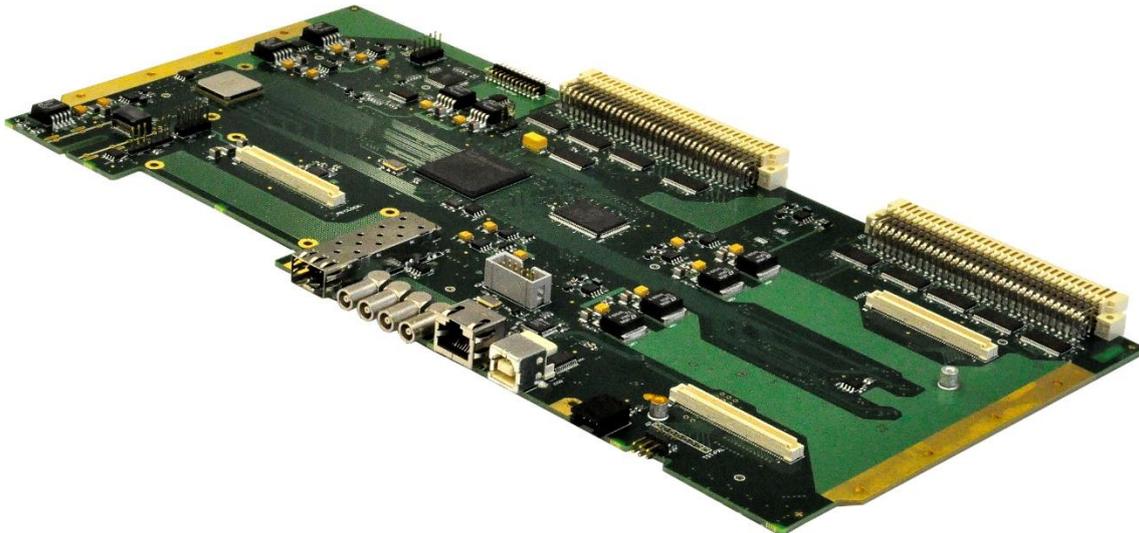


Figure 1: The DRM2 board

3 DRM2 tests and measurement results

We tested the DRM2 both with the CRU and the C-RORC [7] readout cards with two different goals:

- with the CRU, we measured the quality of the received clock;
- with the C-RORC, we focused on the readout performances with the DRM2 board inserted in an almost full VME crate.

The following two sub-sections give results related to these measurements.

3.1 Clock jitter measurements with CRU

We built an electronics setup with the TTC-PON [8], providing the clock to a CRU board, which, in turn, sent the clock to the DRM2. We measured the clock characteristics with a LeCroy SDA3010. The measured RMS period jitter was as low as 8.2 ps on the GBT Phase Shifter single ended clock. The RMS period jitter on the GBTx Test Clock Output (TCO) was 13 ps, as measured on a LEMO connector. In all cases, the measured clock jitter is very good, even exceeding the high-quality clock from LHC, which is currently being used in the ALICE TOF. We do not expect long term drift on the received clock to be an issue for TOF detector.

3.2 Data readout performances with C-RORC

We made readout performance tests using an almost full crate (8 TRMs) with a DRM2. After checking the correct behavior of the VME bus with single BLT32 and MBLT accesses to the TRM boards via the CONET2 link, we began running data acquisition with a C-RORC, featuring a special firmware implementing a GBTx FPGA core. As stated above, the time budget between two consecutive triggers is 30 μ s. This value needs to be longer than the sum of the following intervals:

1. time interval needed in order to read the HPTDCs and store data words in the TRM buffers: this time interval has a constant part of 4.025 μ s and a variable part, which depends upon the number of data words, i.e. occupancy;
2. time interval needed to read all the 8 TRMs one at a time, until all the data are stored into the DRM2 SSRAM;
3. time interval required to send data to the CRU through the GBTx link.

As shown in Fig. 2, we measured the 1+2 time intervals with different values for the number of data words per TRM. The measured time is lower than 20 μ s even for 26 words per TRM, which is much higher than the expected occupancy for RUN3-RUN4. The occupancy we expect for Pb-Pb interactions in 30 μ s is around 15 words per TRM, so we are confident of reading out with continuous triggers at 33 KHz without problems.

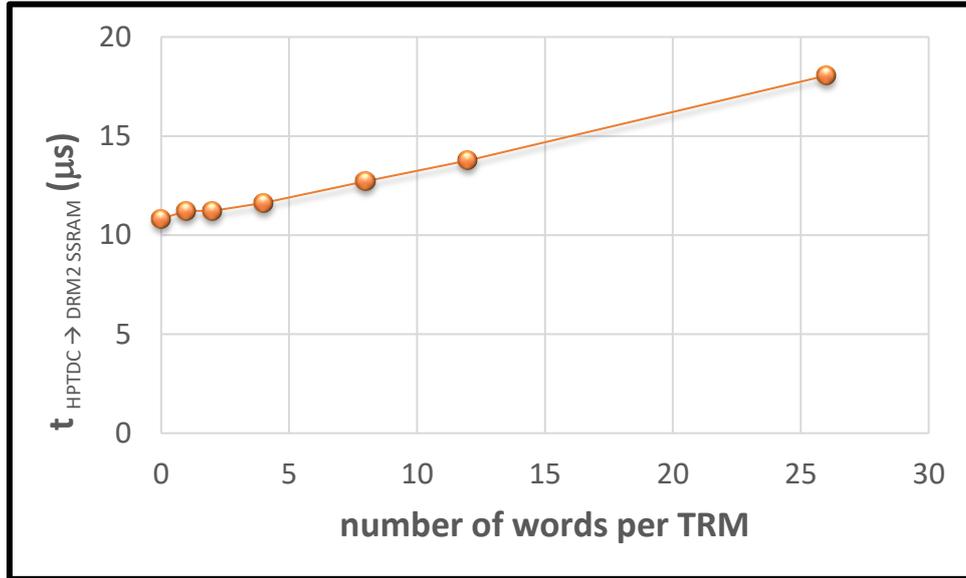


Figure 2: TRMs readout time versus occupancy

4 Conclusions

We have presented the design details of the DRM2 board, together with the measurement results of the performances, obtained working with DAQ cards (CRU and C-RORC), for what concerns both the received clock quality and the data transmission bandwidth towards the DAQ. From the results of the tests with the CRU, we have the proof that the TOF HPTDCs can use the clock received through the GBTx link, since it is a high-quality clock with low level of RMS jitter (O(10 ps)). From the results of the tests with the C-RORC, we are confident to work in continuous readout mode at 33 KHz without running into the busy condition.

We are planning to further test the system before launching the production of the 72 boards needed for the experiment.

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