PoS PROCEEDINGS OF SCIENCE

Effect of Gamma Irradiation on Leakage Current in CMOS Read-out Chips for the ATLAS Upgrade Silicon Strip Tracker at the HL-LHC

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The increase of the leakage current of NMOS transistors in detector readout chips in certain 130 nm CMOS technologies during exposure to ionising radiation needs special consideration in the design of detector systems, as this can result in a large increase of the supply current and power dissipation. As part of the R&D program for the upgrade of the ATLAS inner detector tracker for the High Luminosity upgrade of the LHC at CERN, a dedicated set of irradiations have been carried out with the ^{60}Co gamma-ray source at the Brookhaven National Laboratory. Measurements will be presented that characterise the increase in the digital leakage current in the 130 nm-technology ABC130 readout chips. The variation of the current as a function of time and total ionising dose has been studied under various conditions of dose rate, temperature and power applied to the chip. The range of variation of dose rates and temperatures has been set to be close to those expected at the High Luminosity LHC, i.e. in the range 0.6 krad$\,$h^{-1} - 2.5 krad$\,$h^{-1} and between -10 °C and +10 °C. Two of the chips under test were pre-irradiated with high doses of X-rays at Rutherford Appleton Laboratory. The results show the dependence of the leakage current with the parameters under study and provide valuable information for the understanding of the underlying mechanisms responsible for radiation damage in transistors and detector readout chips.

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1. Introduction

At the core of the ATLAS detector upgrade for the High Luminosity LHC (HL-LHC) is a new sub-detector for tracking charged particles, the Inner Tracker (ITk) [1]. The ITk silicon strips will be read out by the 130 nm-CMOS-technology ABCstar chips, which must withstand dose rates of total ionizing radiation in the range of 0.6 krad$\,$h^{-1} - 2.5 krad$\,$h^{-1} from LHC collisions and will be operated at sub-zero temperatures. During the 2015 *pp* collisions at $\sqrt{s}$ = 13 TeV, a significant increase of low-voltage (LV) current was observed in the read-out chip of the innermost pixel layer of the ATLAS detector, the Insertable B-Layer (IBL) [2]. This read-out chip, the FE-I4, is designed in 130 nm CMOS IBM technology as is the ABCStar read-out chip. Previous work [3, 4] has identified the cause of the leakage current caused by total ionizing dose (TID) to be due to the charge state of two types of point defects. The first is an oxygen vacancy in the oxide near the Si-SiO_2 interface which traps holes (positive charge) and produces leakage between the source and drain of a parasitic transistor structure. The second is the creation of dangling silicon bonds at the same Si-SiO_2 interface which in an NMOS structure traps electrons and opposes the effect of the trapped holes. During irradiation, the trapped positive charges concentration increases first, followed at larger doses by increases in the trapped electron concentration. This causes the leakage current to increase, reach a maximum at around 1-2 Mrad, and then decrease (TID current bump). This phenomenon, which is dose rate and temperature dependent, needs special consideration for the design of the ITk detector system, as this can result in a large increase of the sub-system's power consumption resulting in additional heat and reducing the overall reliability and performance of the detector. To quantify the dependency of the current increase on dose rate and temperature, several irradiation were performed on both the FE-I4 and the ABC130[1] read-out chips. Among the results of these irradiation campaigns by the ATLAS IBL and ITk Collaborations, two are particularly interesting: at a given dose rate, a higher temperature leads to a lower LV current increase, and at a given temperature, a higher dose rate leads to higher LV current increase. These results can be found in Ref. [1] and [5]. These studies were performed mostly using X-ray sources, with high dose rates (i.e: $\sim$100 krad$\,$h^{-1}). To test this behavior at typical HL-LHC conditions for the ITk Strip detector (i.e. dose rates and temperatures) a set of measurements on the ABC130 chip was made utilizing a ^{60}Co gamma source at Brookhaven National Laboratory (BNL).

2. Experimental setup

In order to characterise the TID bump, an experimental setup was developed in which leakage current could be studied under different experimental conditions, i.e. dose rates, temperature and chip biases. The experimental apparatus comprises several thermally insulated boxes, each containing an ABC130 chip in N_2-dried air, temperature and humidity sensors and a remote-controlled thermo-electrical cooler. A total of 7 ABC130 read-out chips have been irradiated in 2 irradiation campaigns which are defined in this document as BNL-run1 and BNL-run2. Among the 7 read-out chips, two have been pre-irradiated while unpowered, at Rutherford Appleton Laboratory (RAL) using X-rays at a dose rate of 0.85 Mrad$\,$h^{-1} for 10 hours, i.e. reaching a TID of 8.5 Mrad, in

[1] As the final chip ABCStar was not available, all R&D studies presented in this document are based on the prototype chip ABC130, implemented in the same underlying CMOS 130 nm technology

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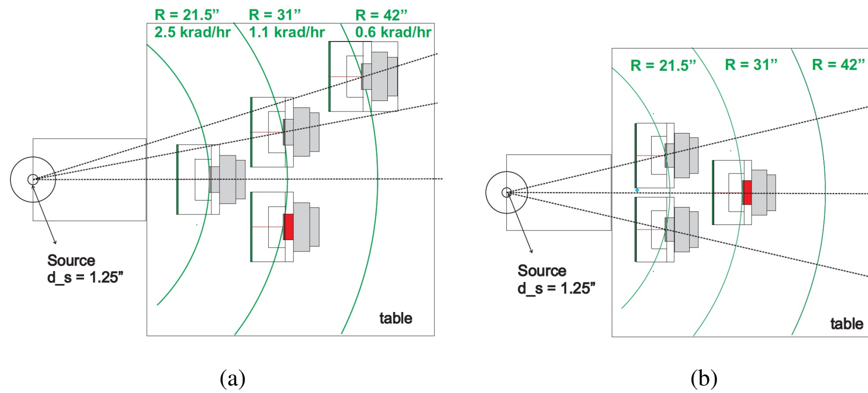

Figure 1: Sketches of BNL experimental setups for BNL-run1 (a) and BNL-run2 (b). Dose rates are reported along with the distance values of the chips from the ^{60}Co source. The red boxes indicate the pre-irradiated ABC130 chips.

order to study the effect of radiation on pre-irradiated devices. The configuration for the two BNL runs is shown in Fig. 1 with the pre-irradiated boards marked in red. During BNL-run1, 4 read-out chips were exposed to gamma-rays of 3 different dose rates: 2.5, 1.2 and 0.6 krad h^{-1}, while during BNL-run2 3 ABC130 chips were irradiated at 2.5 and 1.2 krad h^{-1} as illustrated in Fig. 1. During BNL-run1 the initial temperature was set to -10 °C for all the ABC130s. During BNL-run2 the two chips irradiated at highest dose rate were set to temperatures of -10 °C and +10 °C while the chip at the intermediate dose rate of 1.2 krad h^{-1} was irradiated at a temperature of -10 °C.

3. Results

The results of the BNL irradiation campaign reproduced the general observations by other experiments, i.e. an increase in leakage current from baseline values (i.e. prior to irradiation), followed by a gradual decrease after a peak is reached until a baseline value is reached. As shown in Fig. 2a data confirm the dependence of the LV current increase from the dose rates observed previously at high dose rate, where higher dose rates induce higher LV current increases. The TID at the current peak is around 0.8 Mrad for all the chips allowing for a 10% precision in the dosimetry measurement. The dependence of the radiation-induced leakage current on the voltage bias on the chip has been investigated by switching off the power for ∼3 days during the irradiation (red curve in Fig. 2a): when the chip was powered back on, the leakage current went suddenly down, close to levels prior to irradiation, then slowly increased to follow again the original curve in about 15 days. This result is consistent with what is reported from IBL data.

In order to study the dependence of the leakage current on temperature, the temperature was raised, from -10°C to +10°C for two of the four chips irradiated during BNL-run1. This variation was done at about 1.5 Mrad of TID, i.e: on the down-fall of the LV current. As a result of this operation, after a transient period of sudden current increase, the current unexpectedly decreased resuming the original curve. This trend is apparently inconsistent with the previous measurements where higher temperatures resulted in lower LV current increase.

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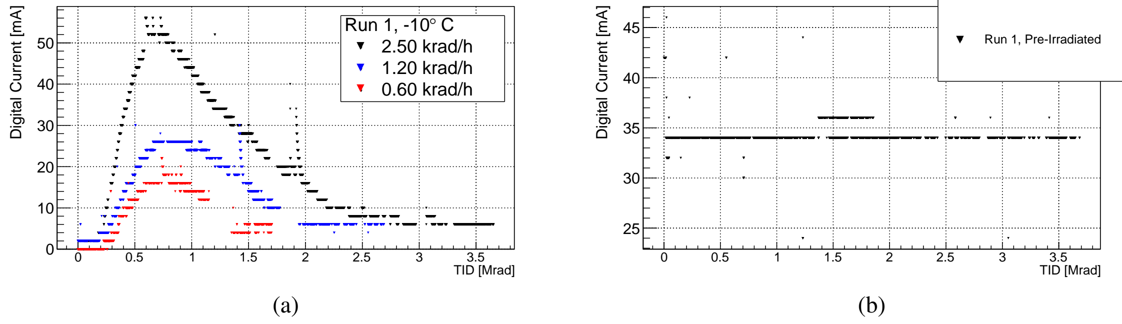

(a)

(b)

Figure 2: Current change in ABC130 chips as a function of TID during BNL-run1 for (a) non pre-irradiated (the initial-state current baseline values are subtracted) and (b) pre-irradiated chips.

The leakage current versus TID for the pre-irradiated chip is shown in Figs. 2b. The current is constant at the initial value of 34 mA: no TID bump has been observed up to 7 Mrad.

The goal of BNL-run2 was to confirm the BNL-run1 result on the pre-irradiated chip and to investigate further the dependence of the leakage current on temperature. In this run configuration, two of the boards were operated at two different temperatures while being exposed to the same dose rate (Fig. 1b). Results are shown in Fig. 3. Fig. 3a shows that the current peak for the chip at +10 °C is lower than the one at -10 °C in agreement with observations of previous experiments. This result together with BNL-run1 result indicates that the effect of temperature on current is different depending on whether the temperature is set at the start of the irradiation or on the current down-slope after the peak. As shown in Fig. 3b the BNL-run2 measurement of the pre-irradiated chip confirms BNL-run1 results: the leakage current is constant at 32 mA throughout the run, up to 3 Mrad. The data in Fig. 3a show also another unexpected result: the current peak value of the chip irradiated at 2.5 krad and at -10 °C is half the value than the one under the same experimental condition in the previous run (see Fig. 4). This difference between the two sets of measurements is an indication of a batch-to-batch effect: after further investigations it has been found that the ABC130 chips irradiated in BNL-run1 and BNL-run2 belong to different fabrication batches[2].

4. Interpretation and conclusions

Two sets of irradiations of ABC130 read-out chips for the ATLAS strip ITk detector have been conducted at BNL using a ^{60}Co source of gamma-rays. Measurements of the radiation-induced leakage current as a function of TID at HL-LHC dose rates and different temperatures have been carried out. These measurements provide important inputs to accurately predict the ITk subsystem's power consumption as well as to a better understanding of the underlying physics mechanisms of radiation effects in CMOS red-out chips. Some unique features have been observed. A dependence of the current increase on temperature has been confirmed only when the temperature

[2]This batch-to-batch dependence of the current has been later on verified by colleagues at RAL by irradiating several ABC130 chips from the same two batches as used in the BNL measurements reported here. In addition, a wafer-to-wafer dependence has been observed.

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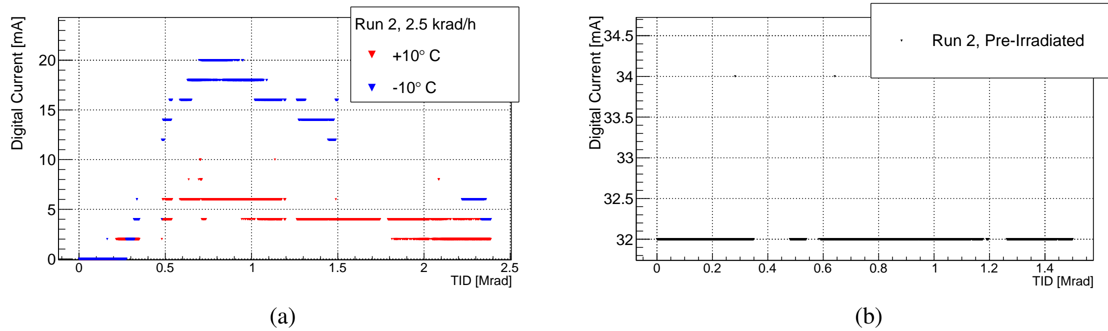

(a) (b)

Figure 3: Current change in ABC130 chips as a function of TID during BNL-run2 for (a) non pre-irradiated (the initial-state current baseline values are subtracted) and (b) pre-irradiated chips.

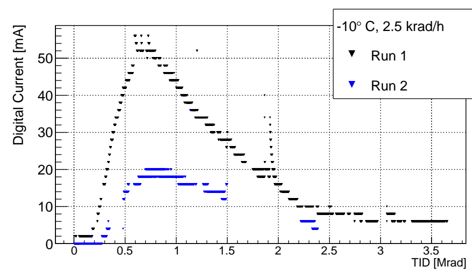

Figure 4: Comparison between the two ABC130 chips under the same conditions (i.e: 2.5 krad h^{-1} at T = -10 °C) in the two BNL irradiation runs.

is set from the start of the irradiation: this effect may provide insight on the temperature dependence of some of the competing underlying processes. Furthermore, a batch-to-batch dependence of the digital current has been observed, which makes the modeling of radiation effect and the prediction of the maximum leakage current value even more complex. However, the constant current of pre-irradiated chips as a function of radiation doses indicates a possible way to eliminate radiation-induced leakage current and avoid the TID bump during ABC130 chips operations at HL-LHC.

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