PROCEEDINGS OF SCIENCE

Readout Electronics System of the CASCA Front-End Chip for the TPC Based X-Ray Polarimeter

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The CASCA is a 32-channal readout ASIC designed for the TPC based X-ray Polarimeter. We propose a prototype Readout system of the CASCA chip for the XTP. The system mainly consists of three kinds of modules. The ASIC cards, mounted with CASCA chip, are designed for sampling XTP signals. The Adapter card, edged-mounted with the ASIC card, is in charge of digitizing the output from ASIC card and driving it. The Main Controller card provides 8 channels for 8 Adapter cards based Serial-RapidIO protocol at 6.25Gbps bandwidth, and it transmits data through 10 Gigabit Ethernet, therefore 256 electronics channels are achieved. The readout system can be tailored to specific sizes to adapt to the experiment scales and readout requirements.

Topical Workshop on Electronics for Particle Physics
11 - 14 September 2017
Santa Cruz, California

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PoS(TWEPP-17)104

1. Introduction

Micro-pattern TPC (Time Project Chamber) based X-ray polarimeter (XTP) has been demonstrated in recent years for its main advantage of releasing the competition between absorption depth and drift distance [2]. It measures two dimensional photoelectron tracks generated by the incident X-ray photons with one dimensional strip readout. The other dimension is calculated by the drift time from the signal waveform. The polarimeter focuses on the X-ray energy of 2-10 keV whose track length is only several millimeters, and 100 um track resolution, fast sampling rate (20MSPS) is required. All these characters leads to high density and low power readout electronics.

A new dedicated ASIC named CASCA, which integrates 32 channels in 0.18 um CMOS technology, has been designed by Department of Engineering Physics in Tsinghua University. Each channel of CASCA integrates the front-end part and the SCA, the former for amplifying and shaping and the latter for sampling [3]. The ASIC finally outputs a pair of differential signals from 32-channels. And its valid sampling rate is designed for 40Msps and the readout frequency is 5MHz. Analog output from CASCA need to be digitalized and transported by the readout system. The detailed design for the readout system will be presented in this paper.

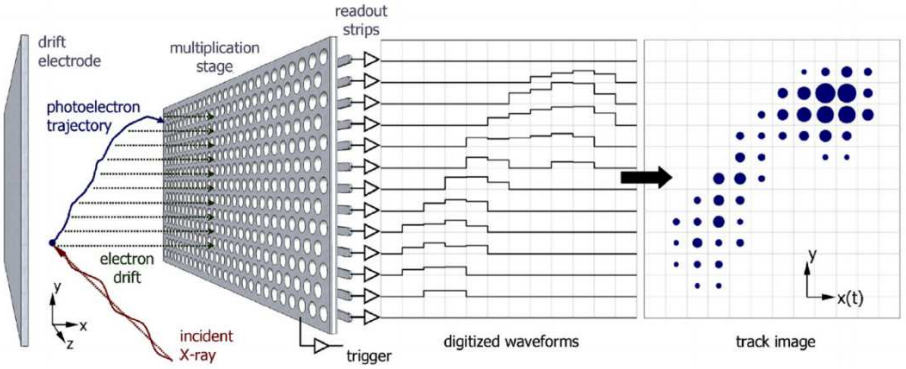

Figure 1: Simplified schematic diagram of the XTP

2. System Architecture and Specifications

2.1 Architecture of the readout system

The architecture of the readout electronics is illustrated in Fig 2. It mainly contains the ASIC card, the Adapter card and the Controller card. Multiple controller cards with one clock-trigger card transmit data to Ethernet switch by the network cables.

One basic controller card could provide 256 electronics channels. The Adapter card edged-mounted with Frond-end card is near to the detector and sampling waveform. The ASIC card is designed for one CASCA ASIC providing 32 electronics channels. And the CASCA ASIC records analog transient signals from 32 electronics channels of the XTP detector. The trigger of the ASIC could be from outside or by itself. Each adapter card receives the analog signal from the ASIC card. And in a way of "Several-in-One", 8 adapter cards are connected to one Main controller card through a Mezzanine card with 8 HDMI2.0 cables. Similarly, several controller cards link to the Ethernet Switch with several network cables in parallel.

A synchronous clock and trigger card is designed to ensure the whole readout electronics system operating synchronously. The clock signal is generated with a local oscillator on Clock and Trigger module and fanned out to all the Controller cards.

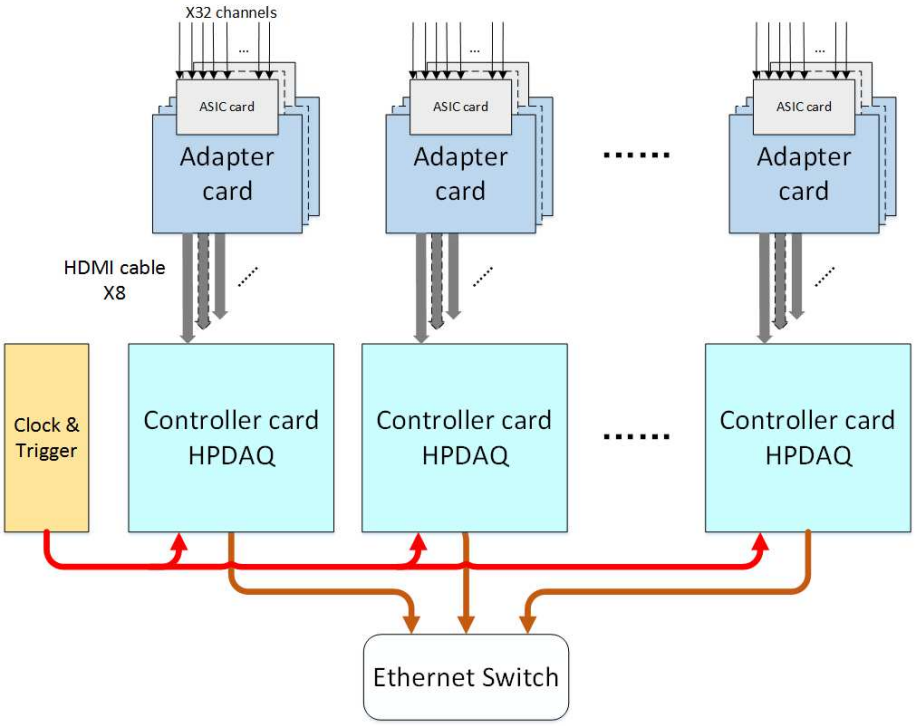

Figure 2: Architecture of readout electronics system

2.2 ASIC card and Adapter card

The ASIC card named CASCA card is designed for configuring the CASCA chip and transferring the output signal from the CASCA chip. An ultralow noise, high performance differential amplifier is adopted in the CASCA card to provide the rail-to-rail output for the high precision ADC (Analog to Digital Converter) in the Adapter card. The CASCA is a high density and low power readout ASIC and it works on the specific control signals provided by a small FPGA chip in the Adapter card.

The Adapter card[1], edged-mounted with the CASCA frond-end card by a double header, is in charge of digitizing the output from the CASCA card and driving the ASIC. A FPGA chip and a multi-output clock generating chip are mounted on the Adapter card. The FPGA chip provides necessary logic signals for the CASCA ASIC and is responsible for packaging the digital data from 32 channels. The clock generator AD9517 is configured to meet the requirement of the 40MHz sampling clock and the 5MHz readout clock. Since the ASIC card and the local ASICs need particular power supplies which were regulated by the local LDOs, the initial voltages were supplied via the HDMI2.0 cable from the Main controller card. The schematic of the Adapter card is shown in Fig 3.

To meet the bandwidth of dataflow between the Adapter card and the Main card, we selected a Xilinx Artix-7 FPGA chip which provides a quad of the GTP transceiver. With the help of the

Serial RapidIO Technology and HDMI2.0 cable, the bandwidth could achieve the maximum of 6.25Gbps which is over the requirement of the Adapter card. The data transfer through the Serial RapidIO protocol realized by the Logic IP Serial RapidIO Gen2 Endpoint Solution in the FPGA.

Trigger and Clock also are transmitted from the Controller card by the HDMI2.0 cable in differential mode.

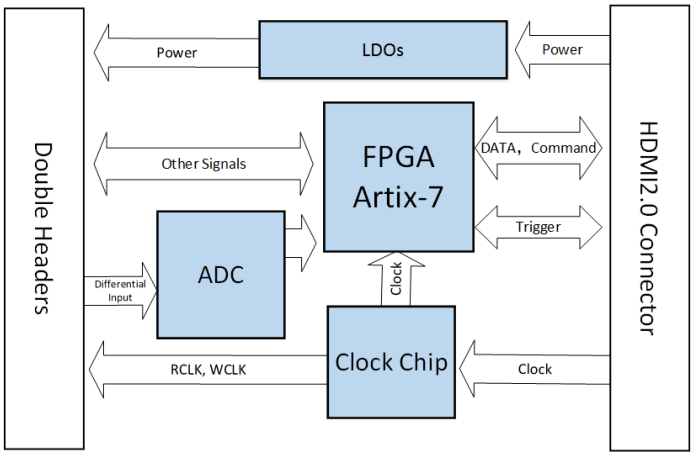

Figure 3: Schematic of the Adapter Card

2.3 Clock and Trigger card

To ensure the whole readout electronics system operating synchronously. It contains the generation and distribution of the clock and trigger signals.

The clock signal is 125MHz, which is generated with a local oscillator. A PLL chip is used to filter out the jitter noise and fan out the clock signal to the clock generating chip and the GTP module on the adapter cards with the help of the Controller cards.

In this readout system, there are three kinds of trigger: self-trigger, soft-trigger and outer-trigger. Self-triggers are generated by the CASCA ASIC. Soft-triggers are the software trigger in DAQ system. And the outer-triggers come from the Clock and Trigger card. The card receives the analog signals and generates trigger signals, which contain the analog energy sum and the over-threshold channels information.

2.4 Main Controller card

The Main card named HPDAQ2, has a high-performance FPGA chip to provide the logic resource and I/O interfaces, and 2GB DDR4s as the data buffer.The Main Controller card is shown in the right-top of the Fig 4.

The card adopts a Xilinx Kintex UltraScale FPGA device in 20nm technology. It mainly consists of four HP I/O Banks, two HR I/O Banks, and three GTH Quads. And four high-capacity DDR4s are used to store data with the speed of 2400MHz.

FPGA device provides three GTH Quads, each containing four MGTHs with the speed of 16.3Gb/s respectively. One of the MGTHs is used for 10 Gigabit Ethernet by the SFP+ module. And the others connect to the FMC connector for the data transmission through the Serial RapidIO protocol realized by the Logic IP core in the FPGA.

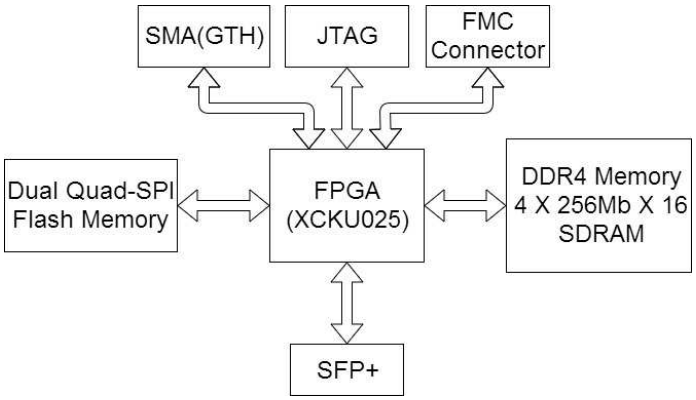

Figure 4: Schematic of the Controller Card

3. Summary and Acknowledgement

A prototype of XTP detector readout system using a CASCA asic has been designed. And this readout electronics system is flexible to apply in the XTP. A Master card is able to support 256 or more detector channels, and a large number of the Master card could be assembled in parallel to meet the requirement of the large XTP.

Finally, we acknowledge the support from the NSFC of China (Grant Number 11505074).

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