PROCEEDINGS OF SCIENCE

Design of the new front-end electronics for the readout of the upgraded CMS electromagnetic calorimeter for the HL-LHC

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The Compact Muon Solenoid detector was originally designed to operate for about ten years, for LHC instantaneous luminosity up to $1 \cdot 10^{34}$ cm^{-2} s^{-1} and integrated luminosity of 500 fb^{-1}. The High Luminosity LHC will increase the instantaneous luminosity by about a factor of 5 from current levels and CMS will accumulate an integrated luminosity of 3000 fb^{-1} by about 2035. With such high luminosity the electromagnetic calorimeter of CMS will have to cope with a challenging increase in the number of interactions per bunch crossing and in radiation levels.
The front-end readout electronics will be completely redesigned, with the goals of providing precision timing, low noise and added flexibility in the trigger system. It will use a faster pre-amplifier, increase the sampling frequency from 40 MS/s to 160 MS/s and implement a trigger system that resides entirely off-detector.

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1. Introduction

The High Luminosity LHC (HL-LHC) will provide an instantaneous luminosity 5 times the one of the current LHC. The primary driver of the ECAL upgrade is the trigger requirement for an increase of the trigger latency from about 6.4 μs in the legacy system to a maximum of 12.5 μs, and a Level-1 trigger rate of up to 750 kHz compared to the current 150 kHz. These are both mandatory at HL-LHC in order to maintain the physics performance of CMS while exploiting the higher luminosity. Moreover the HL-LHC conditions are a significant challenge to both detector and electronics and performance because the increase in the accumulated radiation dose and fluence levels will imply significant loss in crystal light transmission and photo-detector performance.

2. ECAL on-detector readout electronics

To provide the desired energy resolution over the full range of the signal events, the front-end readout electronics will be completely redesigned. The readout system time resolution has to be optimized in order to minimize the event pile-up and the impact of signals generated by hadrons directly hitting the avalanche photodiodes (APDs), also called "spikes".

2.1 Current front-end design

Each lead-tungstate crystal is coupled to two APDs connected in parallel to form one analog channel. The APDs are readout by the Very Front-End (VFE) card. Each VFE card has five readout channels consisting of a multi-gain pre-amplifier (MGPA) and a quad-ADC. The MGPA provides three outputs corresponding to different gain values. The three outputs are sampled and converted in a digital representation by 12-bit, 40 MS/s ADCs. The digitized signals from the five VFE cards are sent to a Front-End (FE) card. The FE card forms the trigger primitive for the 5x5 crystal array and contains a digital latency buffer and the primary event buffer. A schematic of the present ECAL on-detector electronics is shown in Figure 1.

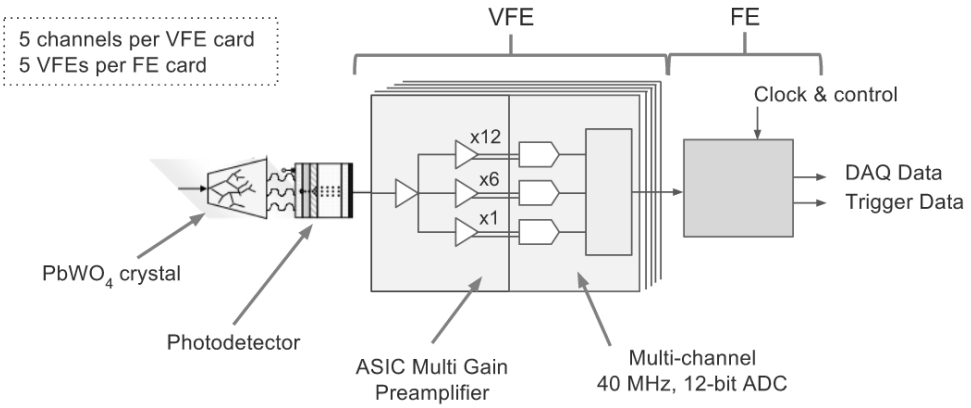

Figure 1: ECAL current on-detector readout chain

All designs were verified to fulfill the required radiation tolerance of 100 kGy, considering the foreseen ten year operation period and an integrated luminosity of 300 fb^{-1}.

2.2 Front-end upgrade

The performance goals of the on-detector readout electronics upgrade require the replacement of the VFE and FE cards. The VFE will be upgraded to increase the timing resolution and the system bandwidth. Such improvement will enhance the detection of the spikes and the separation of pile-up events.

For the first amplification stage a Trans-Impedance Amplifier (TIA) will replace the current charge-sensitive amplifier architecture. The TIA will handle signals in a dynamic range from 50 MeV to 2 TeV. The architecture of the TIA is a Regulated Common-Gate (RCG) which offers a reduced input resistance providing the bandwidth required (50 MHz) with the high input capacitance (200 pF). The TIA will maintain the integrity of the APD signal shape, the signal lasts about 40-50 ns thus 7-8 samples will be extracted per event and two of them will be on the positive edge of the signal. The TIA will provide two gain output which will be digitized by two 12-bit ADCs. A schematic of the upgraded VFE is shown in Figure 2.

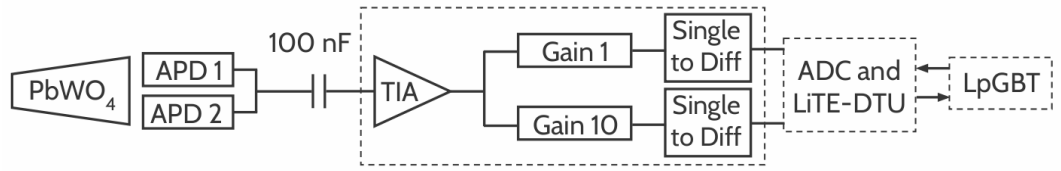

Figure 2: Schematic of the upgrade solution with the TIA and two gain stages

The TIA will be implemented using the 130 nm CMOS technology while the FE digital parts and ADCs will be in 65 nm CMOS technology. The selected technologies are both radiation-tolerant. The data after the digitization and the lossless compression will be sent to a high-speed serial data link based on the LpGBT e-link protocol. The LpGBT optical links will enable us to send all the single crystal data to the off-detector electronics. The off-detector electronics will be upgraded to accommodate the higher transfer rates. It will also integrate the new Level-1 trigger pipeline and the trigger primitive generation off-detector.

3. ADC and Data Transmission Unit

In the electronic readout chain, the preamplifier ASIC is followed by a Data Transmission Unit, named LiTE-DTU. This unit will receive the two analog signals from the preamplifier outputs and will convert them into a digital representation. The LiTE-DTU comprises three main units: the ADCs, the data selection and compression logic and the serializer.

3.1 ADC

The ADCs will sample at 160 MS/s with 12 bit resolution in order to cover the range up to 200 GeV with 50 MeV resolution for the high gain preamplifier output, and up to 2 TeV with 500 MeV resolution for the low gain output. Such requirements are very stringent that can be meet only using an advanced technology node (65 nm or lower) for the ADC design. The ADC will be designed by an external company and the design will be based on successive approximation architecture. Table 1 summarizes the ADC requirements.

Sampling frequency:	160 MS/s	INL:	1.5 LSB
Resolution:	12 bit	DNL:	0.9 LSB
Supply voltage:	1.08 V - 1.32 V	ENOB:	10.2 bit
Analog input bandwidth:	50 MHz	SNDR:	63 dB
Temperature range:	-20 °C ÷ 85 °C	SEU:	TMR protection
Radiation tolerance:	100 kGy	Technology:	CMOS 65 nm

Table 1: ADC requirements

3.2 Data Transmission Unit

The data selection and compression logic receives two streams of 12-bit data at 160 MHz and controls the output serializers. The two ADCs continuously send samples to two FIFOs, which are used to implement the sample selection algorithm with look-ahead capability. The unit selects data from the ADC connected to the high gain input, unless at least one of the samples in a time window around the current sample is saturated. In this case it selects the data from the low gain input. A separate bit is added in order to specify whether the sample is from the high or the low gain.

Since no zero suppression is foreseen in the VFE-FE section, the amount of data to be transmitted will be large. Simulation studies show that the probability of an event with more than 6 bits is below $2.4 \cdot 10^{-4}$. The data rate will thus be significantly reduced by performing a lossless compression. The stream of selected data samples is therefore encoded in variable length words with an Huffman algorithm. This algorithm can provide a significant data reduction and thus decrease the number of optical fibers required for data output. A simplified schematic of the LiTE-DTU ASIC is shown in Figure 3.

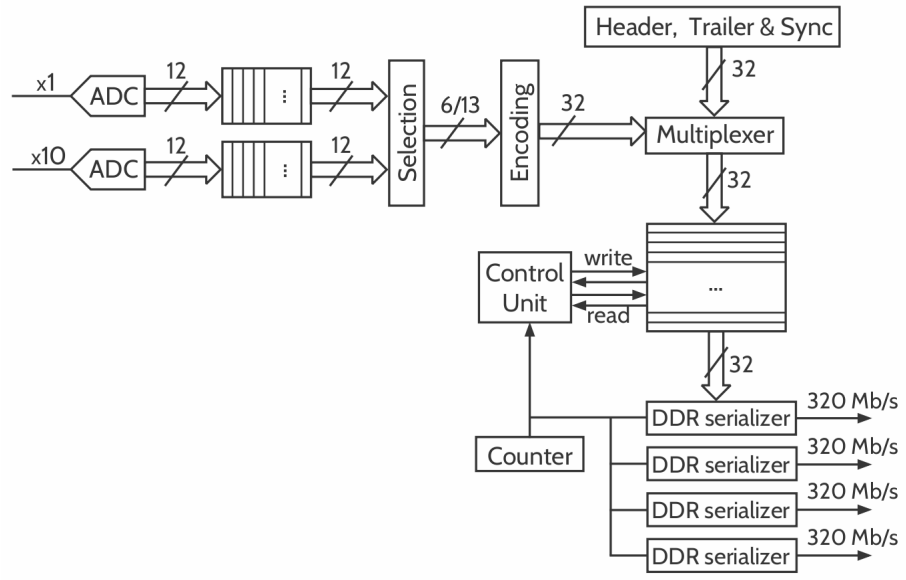

Figure 3: Schematic of the ECAL Data Transmission Unit

A possible implementation of Huffman coding with a data format based on 32 bit words is shown in Figure 4. Samples with less than 7 bits, so-called "baseline samples", are packed in

groups of 5 while the 13-bit samples, named "signal samples", are packed in couples. In either case there are other data formats for the incomplete baseline quintet or signal couple.

Data are organized in frames divided by a frame delimiter which includes the number of data samples collected in the frame, a CRC12 error detection code and a frame number. A synchronization packet is inserted whenever no data are available in order to keep the link active.
The formatted data are inserted into a FIFO, that is used to interface with the high speed serializer.

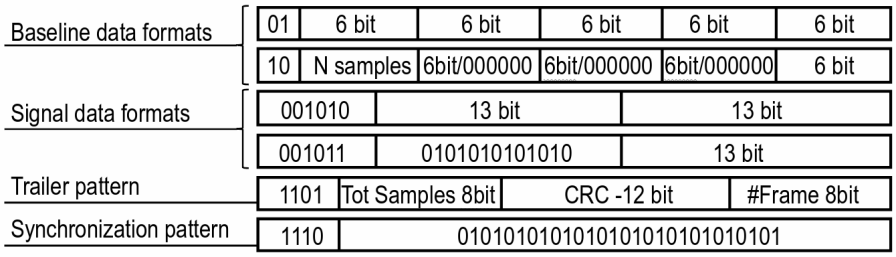

Figure 4: The Huffman coding implementation with 32 bit data words

4. Conclusion

The HL-LHC will provide unprecedented instantaneous and integrated luminosities. Although the lead tungstate crystals and the APDs will continue to be operational and still perform well, there will be an increase in noise, due to radiation-induced dark-currents, and in pile-up events.
The upgrade of the front-end readout electronics will provide precision timing, noise mitigation, added flexibility and enhanced triggering possibilities.

References

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[3] Michael David Planer, *"The CMS electromagnetic calorimeter barrel upgrade for High-Luminosity LHC"*, in proceedings of *TIPP 2014*, PoS(TIPP2014)268 (2014).