PROCEEDINGS OF SCIENCE

# Design studies for the off-detector electronics of the upgraded CMS Barrel calorimeter for the HL-LHC

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After the high-luminosity upgrade of the LHC, the electromagnetic calorimeter and the hadron calorimeter of CMS Barrel must cope with an increase in the number of interactions per bunch crossing and an increase in radiation levels. CMS implements a sophisticated two-level triggering system composed of the Level-1, instrumented by custom-designed hardware boards, and a software High-Level-Trigger. To this end, the off-detector electronics have been redesigned with increased capabilities, exploiting increased granularity of both calorimeters at Level-1. The paper focuses on this new off-detector electronic board design.

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## 1. Introduction

In order for the CMS electromagnetic calorimeter (ECAL) in the barrel region (EB) to support the high-luminosity upgrade of the LHC (HL-LHC), the trigger latency must increase from about 4 $\mu$s to a maximum of 12.5 $\mu$s (or 500 bunch crossings) and the Level-1 trigger rate must increase from 100 kHz to 750 kHz [1]. Therefore, the front-end ECAL trigger tower electronics will be replaced so that they will no longer compute trigger primitives of five-by-five crystals, but will instead provide single crystal sample data of all 25 crystals to the upgraded back-end electronics. The off-detector, or back-end, electronics will then have the responsibility to form the trigger primitives using this higher granularity information. The upgraded back-end electronics will also handle buffering of event data and transmission of selected events to the data acquisition system (DAQ), which is also currently handled by front-end electronics in the legacy system. In order to handle mitigation of the increased noise at the front-end for HL-LHC, the sample rate will be increased four-fold to 160 MHz [1]. Therefore, the upgrade to the back-end electronics will need to handle the roughly 100-fold increase[1] in data being sent off of the ECAL Barrel detector.

Likewise, the CMS hadron calorimeter (HCAL) in the barrel region (HB) must also support the trigger latency and trigger rate increases for HL-LHC [1]. HCAL is currently undergoing front-end electronic upgrades. The upgraded front-end electronics will support these new rates but the HCAL back-end electronics, which cannot currently handle these rates for HL-LHC, must be upgraded.

In order to handle the HL-LHC back-end electronics needs for EB and HB, a new electronics board has been envisioned, which is called the Barrel Calorimeter Processor (BCP) blade. This unified hardware design will be an AdvancedTCA (ATCA) blade and will have the flexibility to support both EB and HB. The BCP will occupy the nexus between the front-end detector electronics, DAQ, Timing and Trigger; it will send timing information to the front-end, receive all sample data from the front-end, calculate the trigger primitives and send them to the Level-1 Trigger (L1T) and buffer the events before sending the triggered data to the DAQ.

## 2. Barrel Calorimeter Processor (BCP) Blade

### 2.1 Philosophy and design

The Barrel Calorimeter Processor (BCP) blade design is based on the Advanced Telecommunications Computing Architecture (ATCA) architecture, which has been chosen as the CMS standard for back-end computing electronics going forward. It is similar to the MicroTCA architecture familar within CMS but provides for over 3x more power and over 3x more board size per blade. This increase in power and board size will be needed for the multitude of optical transceiver channels and high-speed FPGAs used on the BCP. Since ATCA is the standard for CMS, there are many groups with which can be collaborated in order to employ best practices to the BCP.

The BCP will be designed to support a Xilinx UltraScale FPGA in the B2104 package. Currently, the Xilinx Kintex UltraScale XCKU115 is specifically targeted because it contains enough bidirectional 16 Gbps GTH transceivers along with a large number of DSP blocks, which are expected to be needed for building trigger primitives. The XCKU115 meets these requirements without the much higher price tag of other FPGA options. Figure 1 contains a block diagram that is

[1] 25 crystals x 4-fold sampling rate increase

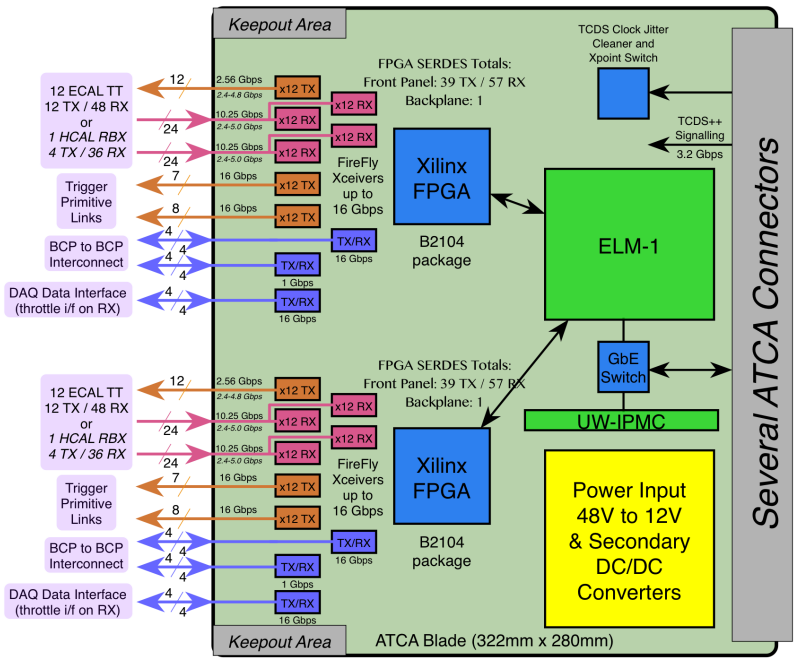


**Figure 1:** Block Diagram of the Barrel Calorimeter Processor (BCP)

roughly to scale showing approximate locations of the two FPGAs along with the fiber transceivers and ATCA support components.

In the block diagram, all of the high speed serial interconnect on the left side of the diagram are optical fiber connections. These are interfaces to the front-end electronics, Level-1 trigger (L1T) system, DAQ interface and also other BCPs in order to handle clustering along a BCP's detector slice boundary. A few high speed interconnects are planned for the ATCA backplane, which are on the right side of the diagram. These backplane interconnects are for timing data from the DAQ and TTC Hub (DTH) and for Gigabit Ethernet for the IPMI controller and FPGA control systems.

Clocks synchronous to the LHC will also be sent along the ATCA backplane from the DTH. The BCP will have a carefully designed clock routing system along with clock synthesizers and jitter cleaners. This will be required to handle the many different clock rates needed for the different high speed serial interfaces.

The BCP is designed so that each of its two FPGAs can receive sample data from 12 ECAL trigger towers (TT) or an entire HCAL RBX. This means that 3 BCPs will be required to cover an entire ECAL SuperModule. With 36 SuperModules in the CMS ECAL Barrel, this means that a total of 108 BCPs will be used for the EB back-end electronics. For the CMS HCAL Barrel, there are a total of 36 RBXes, so only a total of 18 BCPs will be needed for the HB back-end electronics. Much more information on how the front-end detector is partitioned into BCPs can be found in [2].

### 2.2 High Speed Optical Links

Figure 2 shows the interfaces of the BCP configured for ECAL. As can be seen here and in figure 1, the EB front-end will have a total of 24 transmit channels at 2.56 Gbps and 96 receive channels at 10.25 Gbps per BCP. The Level-1 Trigger (L1T) interface and DAQ interface will use

16 Gbps channels; 30 transmit channels for L1T and 8 bi-directional channels based on a higher speed S-LINK protocol for DAQ. For cluster processing, there will be 8 bi-directional channels at 16 Gbps and 8 more at 1 Gbps per BCP.

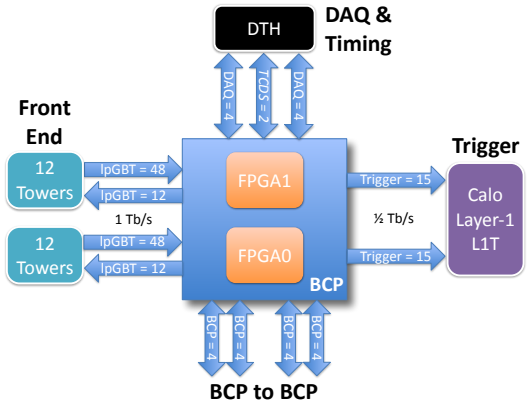


**Figure 2:** ECAL Specific BCP Block Diagram

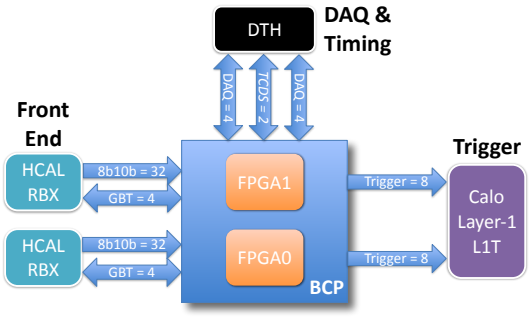


**Figure 3:** HCAL Specific BCP Block Diagram

Figure 3 shows the interfaces of the BCP configured for HCAL. As can be seen here and in figure 1, the HB front-end will have a total of 8 bi-directional channels at 2.4 Gbps, which will be for control, and 64 receive channels at 5.0 Gbps for data per BCP. The L1T and DAQ interfaces are similar to the interfaces for ECAL but with only 16 L1T channels per BCP. HCAL does not require cluster processing so the BCP-to-BCP links are not needed.

To handle the 78 optical transmit channels and 120 optical receive channels of varying link rates, Samtec FireFly™ Micro Flyover Optical Engines [3] will be used. These multi-channel modules are about the size of a small postage stamp and attach to connectors typically on the interior of the blade (hence "flyover"). MPO optical connectors with 12, 24 or 48 channels will be used as the front panel optical interface and will attach to the FireFly™ modules over optical ribbons.

### 2.3 IPMI Controller

In order to support the ATCA architecture, the BCP will need an IPMI controller which monitors the health of the BCP and reports the status to the ATCA crate shelf manager. The shelf manager controls the switching of power to the BCP blades along with other environmental factors. Instead of creating an IPMI controller from scratch, the BCP will use the UW-IPMC that is currently being developed by the University of Wisconsin and can be seen in figure 4. The UW-IPMC has ADCs and digital I/O connected to a Xilinx ZYNQ SoC running a real-time operating system and monitoring application. More information on the UW-IPMC and future plans can be found in [4].

### 2.4 System Control

Although the UW-IPMC provides a microcontroller system for accessing the BCP, it must not be given other tasks that could jeopardize its incredibly important job of continually monitoring the health of the BCP. So another controller is required for reprogramming the UltraScale FPGAs

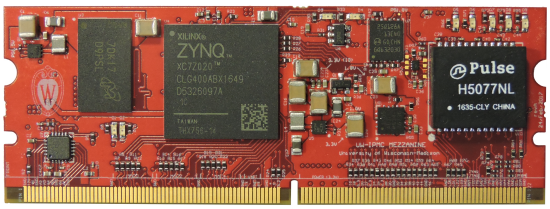


**Figure 4:** Prototype UW-IPMC Module

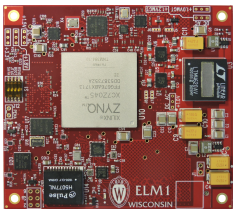


**Figure 5:** Prototype ELM-1 Module

and for configuring and controlling them. Also, this system controller is needed for slow control of other blade components such as the clock synthesizers. For this system controller, the BCP will leverage the Embedded Linux Mezzanine (ELM-1) board, also currently being developed by the University of Wisconsin and can be seen in figure 5. This board is also Xilinx ZYNC SoC based but uses an embedded Linux operating system which will provide a Gigabit Ethernet path to accessing and controlling the main FPGAs on the BCP. A single ELM-1 board can control both FPGAs plus blade slow control. More information on the ELM-1 and future plans can be found in [4].

## 3. Conclusions

In order to effectively operate the CMS detector after the high-luminosity upgrade of the LHC, the ECAL and HCAL Barrel back-end electronics must handle the increase in trigger latency and rate. The presented Barrel Calorimeter Processor (BCP) blade design has been shown how it addresses this exciting epoch of the future LHC.

## 4. Acknowledgements

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