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# Electronics and Firmware of the Belle II Silicon Vertex Detector Readout System

The Silicon Vertex Detector of the Belle II Experiment at KEK in Tsukuba, Japan, consists of 172 double-sided strip sensors. They are read out by 1748 APV25 chips, and the analog data are sent out of the radiation zone to 48 modules which convert them to digital. FPGAs then compensate line signal distortions using digital finite impulse response filters and detect data frames from the incoming stream. Then they perform pedestal subtraction, common mode correction and zero suppression, as well as calculate the peak timing and amplitude of each event from a set of data samples using a neural network.

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## 1. Introduction

At the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, the Belle II experiment [1] will explore the asymmetry between matter and antimatter and search for new physics beyond the standard model. One of its inner tracking systems is the Silicon Vertex Detector [2], which consists of 172 orthogonal double-sided strip sensors arranged cylindrical in four layers (Figure 1) around the collision point to measure the tracks of the collision products of electrons and positrons.

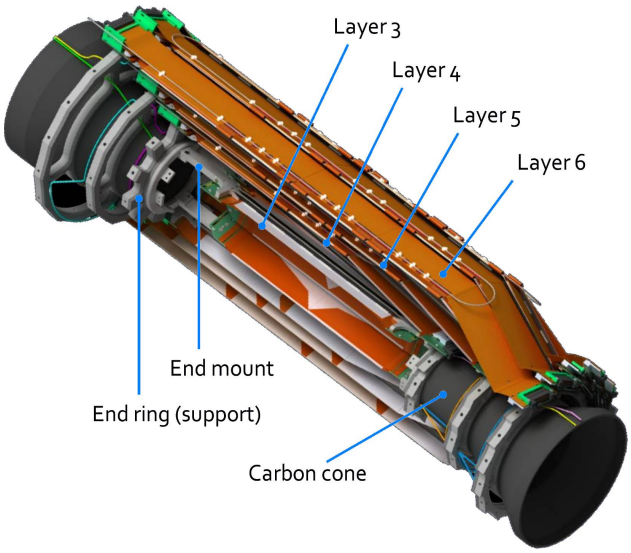


*Figure 1: SVD (inside)*

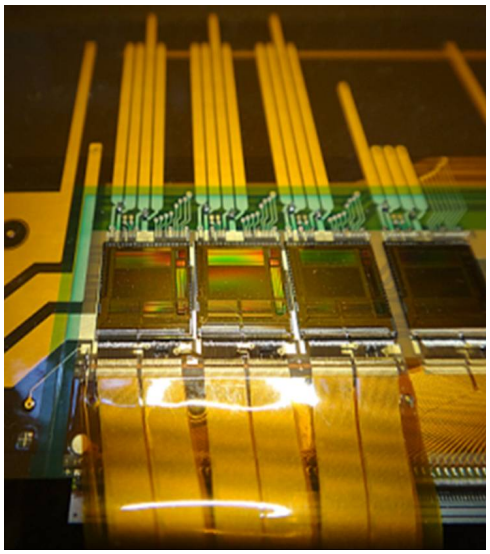

*Figure 2: APV25 ASICs on sensor hybrid*

## 2. Front End Electronics

These sensors are read out by 1748 radiation-hard $CO_2$ cooled APV25 front-end chips [3] (Figure 2), which send one time-division multiplexed differential analog data signal each to eight junction boxes (Figure 3), which power the APV25s using FEAST2 [4] DC/DC-converters over 2.5 meter long cables. The data are sent out of the radiation zone over 15 meter long twisted pair copper cables (Figure 4) to four crates with 48 Flash Analog Digital Converter (FADC) modules [5].

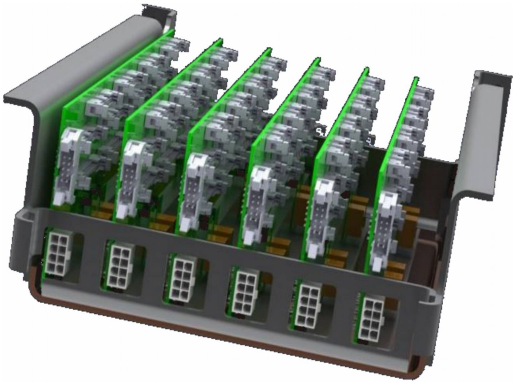

*Figure 3: Junction box*

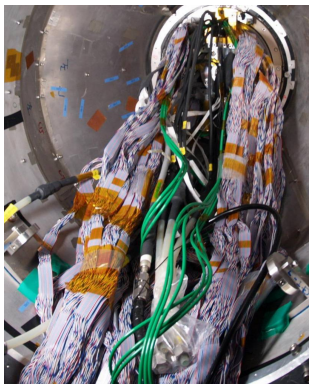

*Figure 4: Cables*

## 3. FADC Modules

These FADC modules (Figure 5) convert the analog data to digital using one flash analog digital converter per APV25 chip. Each module also includes a field programmable gate array (FPGA) chip, namely a Stratix IV GX.

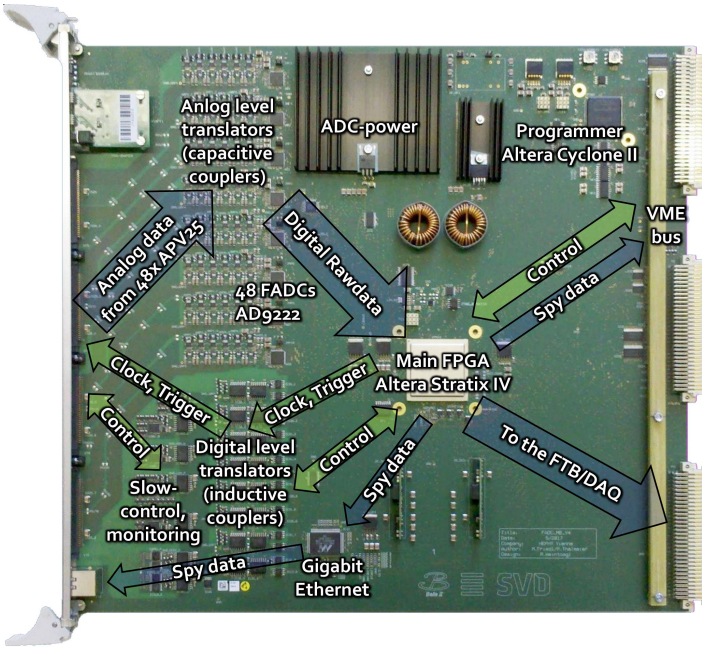


*Figure 5: FADC module*

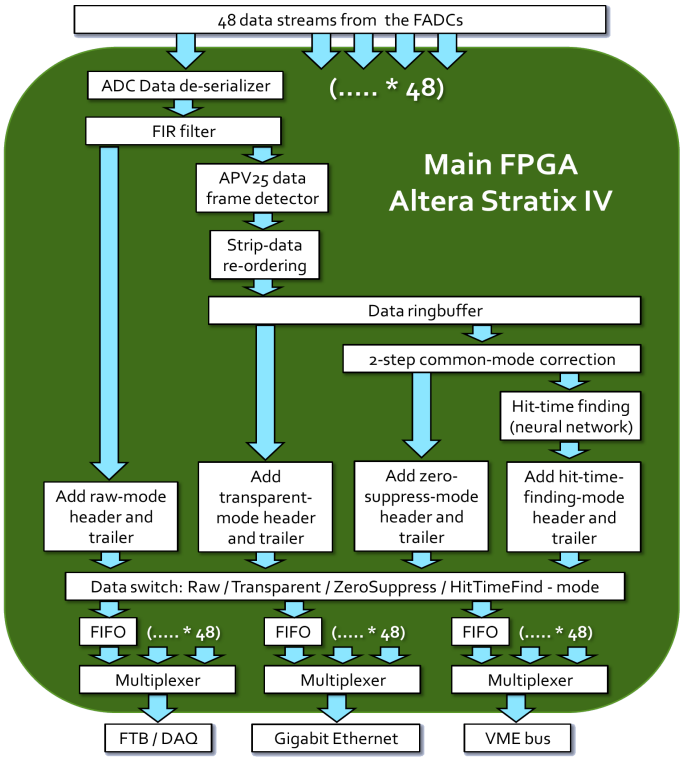


*Figure 6: FADC module data processing*

The data processing part (Figure 6) of the firmware inside this FPGA compensates line signal distortions using digital finite impulse response (FIR) filters and detects data frames in the incoming streams. It reorders the data so that it matches the physical arrangement of the detector, and performs pedestal subtraction to eliminate static offsets, common mode subtraction to remove event-by-event baseline shifts and zero suppression to discard empty strip data. The peak timing and amplitude of each event is calculated from a set of data samples using a neural network in real-time.

The processed data are sent to another detector sub-system, namely the pixel detector, to provide information for timing and the determination of spatial regions of interests, as well as to the Data Acquisition System [6].

## 4. Status and Test results

One segment of the whole SVD readout system has been tested successfully at several test beams at CERN and at DESY, as well as in a persistent setup at DESY for more than six months (2016-12 to 2017-07) with prototypes. Several options in the cabling and hardware have been developed and evaluated [7] to fine-tune the noise immunity and reliability of the SVD system. We had two final candidates for the FADC modules and the corresponding boards in the junction boxes, namely FADC System V3 (Figure 7) and FADC System V4 (Figure 8). The main difference is the cabling concept of the power and data lines from the FADC modules to the detector, where V4 was expected to have much better robustness against possible problems like common mode noise in the power supply cables by avoiding cable loops, which has been confirmed in tests at the HEPHY laboratory.

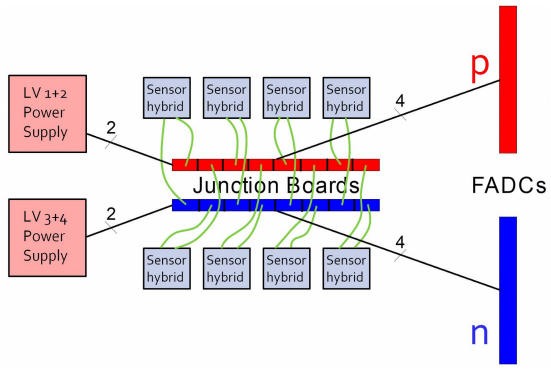


*Figure 7: FADC system V3*

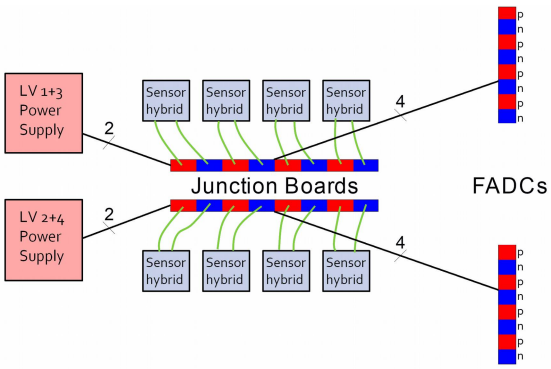


*Figure 8: FADC system V4*

The final decision for FADC System V4 was made in October 2017 at KEK in Japan, where noise injection tests were executed with the final detector structure. V4 again performed much better than V3. For example, white noise was injected into the low voltage power line between a power supply and a junction board using an inductive coupler. Figure 9 shows a color histogram (10.000 samples) of the ADC counts (1024 ADC counts equal to 2 Volts) of the 10-bit DAQ output of the four APV25s on sensor hybrid 4.1.2.1 (Layer 4, Ladder 1, Sensor 2, n-side) using FADC system V3, in contrast to Figure 10, which shows the same of FADC System V4. (The three spikes on strip number 74, 118 and 182 seen in both graphs are known bad silicon detector strips).

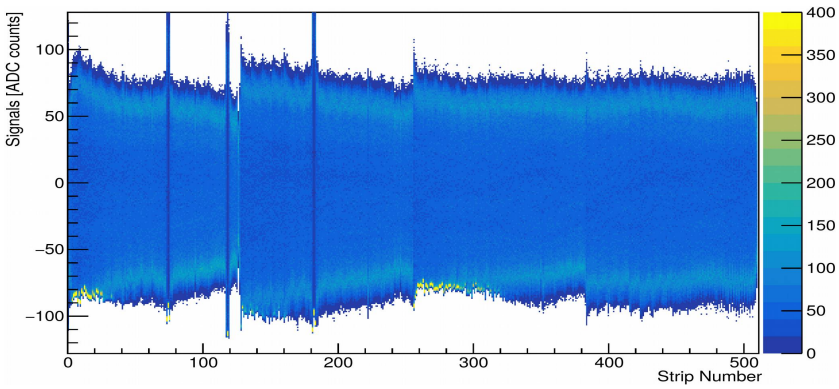


*Figure 9: System noise distribution of Hybrid 4.1.2.1 using FADC System V3*

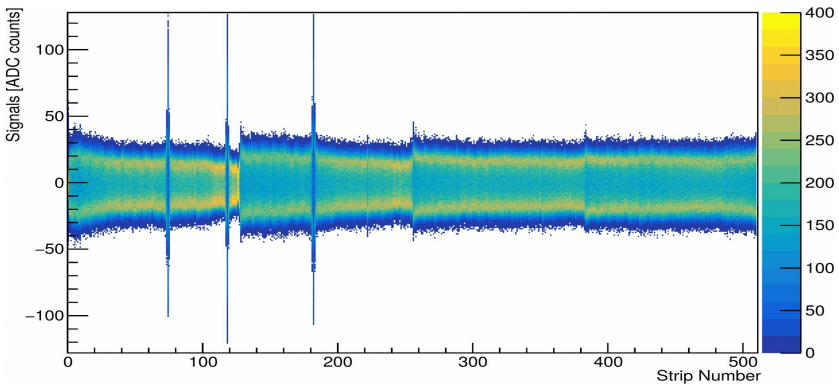


*Figure 10: System noise distribution of Hybrid 4.1.2.1 using FADC System V4*

After this decision, the mass-production and testing of the printed circuit boards has started in Vienna, Austria. The hardware will be delivered to KEK in early 2018 and installed in the second half of that year.

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