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The TrainBuilder Data Acquisition System for the European-XFEL

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The TrainBuilder is an ATCA based data acquisition system developed at the STFC Rutherford Appleton Laboratory to provide readout for each of three Mega-pixel detectors at the European-XFEL Hamburg. Each Train Builder system constructs over 5,000 detector images per second using FPGAs with DDR2 data buffering and an analogue crosspoint switch architecture; thereby processing 10 GBytes/sec of raw image data. The system provides image processing, event formatting and data monitoring. TrainBuilder I/O links to detectors operate using 10 Gigabit UDP protocols implemented in FPGA logic. Four TrainBuilders are now being used to commission detectors for first X-ray beams in autumn 2017.

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1. Introduction

The European XFEL in Hamburg (Eu-XFEL), which started operation in autumn 2017, will generate larger volumes of readout data than any previous X-ray source. The facility delivers trains of up to 2,700 X-ray pulses during short 600 micro-sec spills which are repeated continuously every 100 msec. The Eu-XFEL beamlines are instrumented with novel silicon detectors [1][2][3] each containing a million pixel channels which are segmented into 16 submodules. During initial operation the detectors are capable of capturing diffraction images from up to 510 pulses from each train which are transferred off-detector during the 99 msec inter train gap resulting in a readout rate of 10 GByte/sec.

The TrainBuilder is a custom data acquisition system developed by STFC Rutherford Appleton Laboratory to assemble complete trains of image movies from the detector submodules and deliver them to the nodes of an offline processing farm. It uses a time switched multiplexing architecture which exploits the regular data flows from the detectors. In addition to the main image assembly function the TrainBuilder also provides pre-processing of image data, data formatting and monitoring. In order to achieve this it comprises memory buffers capable of holding complete trains of images, data switch units and 10 Gbps link interfaces to the detectors and farm.

An overview of the Eu-XFEL data acquisition system is shown in (Figure 1). The TrainBuilder hardware is identical for each detector but operates different programmable logic image processing algorithms.

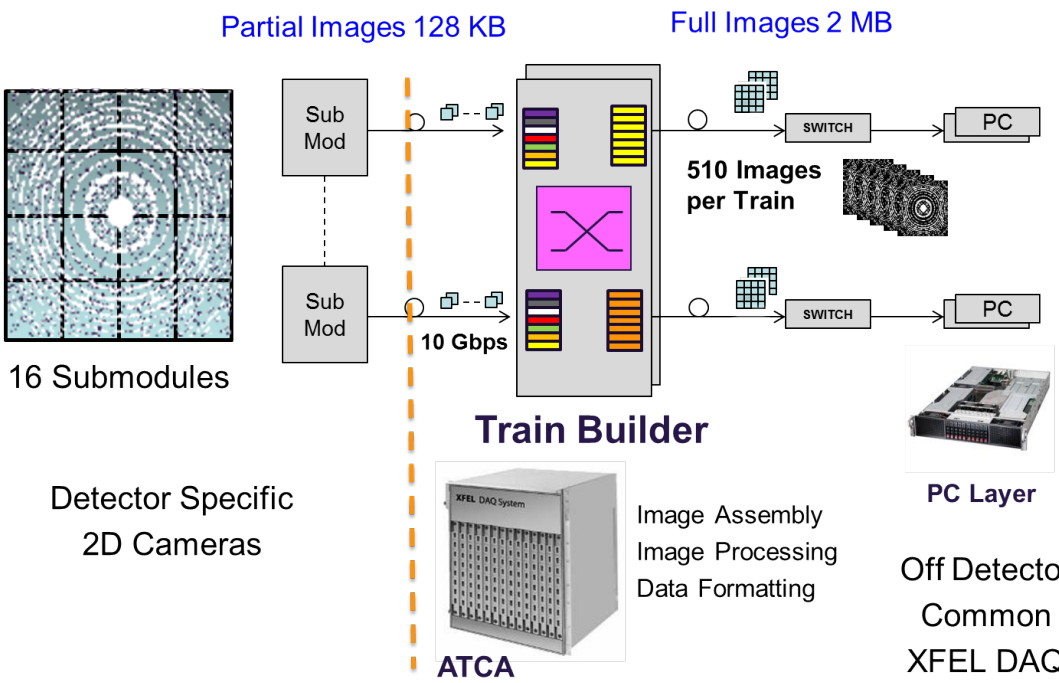

Figure 1: XFEL data acquisition system. Showing detector with 16 partial images from Front-End electronic submodules connecting to TrainBuilder and PC Farm.

2. TrainBuilder System Implementation

The TrainBuilder system is implemented in the ATCA crate standard. The main units are the TB_IO boards. These contain the I/O links to detector and farm, memory buffers and logic modules and a cross-point switch. The processing is implemented with Xilinx Virtex5 FPGAs and they use their unique dual embedded PowerPC processors with DMA offload engines to DDR2 memory to manage the data buffering and formatting. The FPGAs are also programmed with algorithms which perform image processing which are specific for each detector.

Single TB_IO boards were used during commissioning to readout prototype Quadrant detectors consisting of 4 submodules with a total of quarter of a million pixels. This board has been described in an earlier paper [4].

In order to instrument full Megapixel detectors with 16 submodule links four TB_IO boards are required. To handle the increased number of channels a new central switching board TB_SWITCH is added to the system (Figure 2). To interface each TB_IO board to the TB_SWITCH a new ATCA Rear Transition Module RTM is introduced (Figure 2).

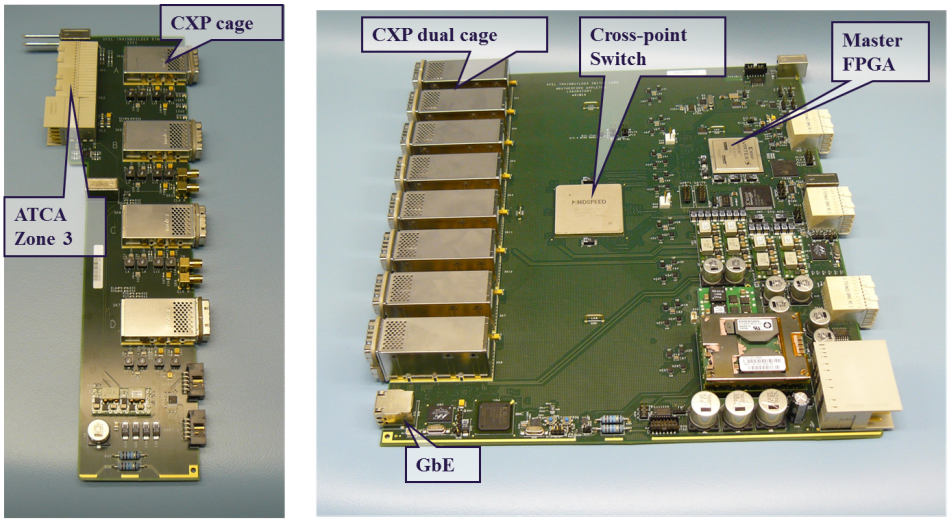

Figure 2: RTM with ATCA connector to TB_IO and CXP cages highlighed (left) and TB_SWITCH board with CXP cages and crosspoint switch (right).

Each TB_IO carries data from 32 Multi-Gigabit Transceiver FPGA links via the ATCA Zone3 rear connector to its associated RTM. The links are distributed on the RTM over 4 CXP cables. The data is transmitted using the Xilinx Aurora serial protocol. The crosspoint switch is protocol agnostic. Handshaking control signals are also transmitted over the CXP cables and these are used to coordinate the operation of the crosspoint on the TB_SWITCH.

The TB_SWITCH board is connected via 16 CXP modules on its front panel. The central component of the TB_SWITCH is a 160x160 analogue crosspoint switch (Mindspeed 21165). The crosspoint is wired to 128 Tx&Rx data links from the 4 TB_IO boards. It can be dynamically programmed to connect any data link on any source to any destination with a switching time of a few microseconds. In normal operation data links will operate at up to 3.125 Gbps, however, the switch can run at up to 6.5 Gbps.

The Master Virtex-5 FPGA manages the crosspoint switch operation using the control signals from the TB_IO boards. For the present application the switch is operated as a barrel shifter with a new switch pattern loaded from memory every 100 msec.

An external PHY connects the Master FPGA to an electrical GbE link on the front panel for PC control. The Master is also connected via the ATCA Zone 2 GbE base channels for communications with an optional ATCA hub card.

A Xilinx Spartan3 FPGA (with embedded Flash memory) provides control of the standard ATCA Zone 1 power. It also monitors temperature sensors which are provided to shut down the board power in the event of a system cooling failure. A Compact Flash card provides configuration storage for the Virtex5 FPGA bit files and associated embedded software files. All digital components are located on a dedicated JTAG chain for Boundary Scan.

3. Status and Conclusions

The correct operation of the TrainBuilder crate system was successfully demonstrated at RAL using internally generated pattern image data at each input. The resulting formatted train data is verified at the outputs on a byte by byte basis. Soak tests are routinely run with the Mega-pixel configuration for several days without error using 2m copper CXP cables.

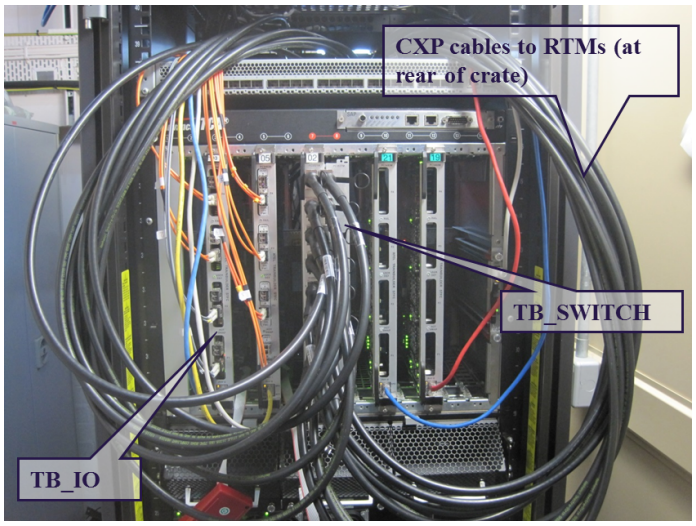

Figure 3: TrainBuilder ATCA Crate for Mega-pixel detector readout. The 2m copper CXP cables (black) connect to RTMs at the rear of the crate (not shown). Two of the TB_IO cards are populated with (orange) fibre connections to detectors.

Four TrainBuilder ATCA crate systems (Figure 3) have been delivered to Hamburg and are currently being commissioned with detectors. The first image processing algorithm for LPD has recently been implemented. The output of data to the PC Farm has also been verified. Two of the three detectors (LPD and AGIPD) are expected to be ready for first X-ray beams in Autumn 2017. The first experiment data taking with the TrainBuilder included in the readout chain is planned for November 2017.

TrainBuilder operation at full XFEL data rates of 510 images per train has been demonstrated satisfying both LPD and AGIPD requirements. Feasiblity studies are under way to increase the

data rate capacity of the existing TrainBuilder firmware to handle the third detector DSSC which is under construction and will be able to capture over 700 images per train.

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