PROCEEDINGS OF SCIENCE

Validation of the front-end electronics and firmware for LHCb vertex locator.

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The LHCb Experiment will be upgraded to a trigger-less system reading out the full detector at 40 MHz event rate with all selection algorithms executed in a CPU farm. The upgraded Vertex Locator (VELO) will be a hybrid pixel detector read out by the "VeloPix" ASIC with on-chip zero-suppression. A complete design overview of the VELO on-detector and off-detector electronics system will be presented. Results on the evaluation of the prototype boards and readout firmware are shown.

Topical Workshop on Electronics for Particle Physics
11 - 14 September 2017
Santa Cruz, California

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PoS(TWEPP-17)121

1. LHCb and VELO upgrade overview

LHCb [1] is an experiment dedicated to search for new physics by studying CP violation and rare decays of b and c quarks.
The whole detector will be upgraded in 2019/2020, at the end of Run-II, with the aim of increasing the instantaneous luminosity to $2 \times 10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, a factor five higher than the current value. In order to do so, it is necessary to improve most ot LHCb subdetectors, remove the current hardware trigger system limit of 1 MHz and also redesign all the front-end and back-end electronics.

Technical improvements on LHCb VELO upgrade

In the framework of the LHCb upgrade is the upgrade of its primary vertex locator (VELO) [2], which will surround the interaction point at LHCb. The upgraded VELO will be a silicon pixel detector, which allows the system to be closer to the interaction point, with active elements at 5.1 mm radial distance to LHC beams (currently this distance is 8.1 mm). Pixel technology (pitch of 55 μm) also improves resolution and therefore the upgraded VELO will have better track reconstruction.
In order to achieve the previously mentioned specifications, a new ASIC has been made, VeloPix, based on the TimePix family of ASICs.
More information about the VELO upgrade is given in Table 1.

Feature	LHCb VELO upgrade
Number of modules	52
VeloPix ASICs	624
Active area	0.12 m^2
HV tolerance	1000 V
Trigger-less readout	~2.9 Tbit/s
Highly non uniform radiation environment	Irradiation profile $4.8\,\mathrm{r}^{-1.89}$

Table 1: Specs of the VELO upgrade

2. VELO on-detector electronics

VELO upgrade will be made up by 52 modules as the one shown in Figure 1.

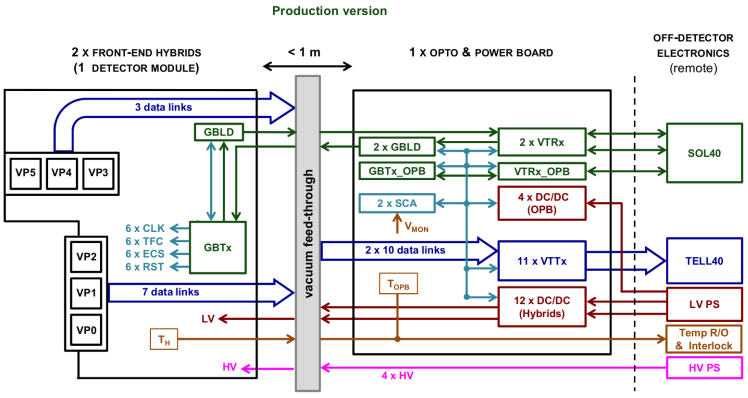

Figure 1: LHCb VELO electronics overview

VELO on-electronics are placed in high vacuum separated from the LHC. Therefore, cooling in this region is challenging, with very low material ~30W per module at -20°C must be dissipated. The solution was use evaporative CO_2 in microchannel silicon substrates instead of cooling pipes.

2.1 VELO module

- Each module is composed of 2 VELO hybrids, one on each side of a silicon substrate. Each side of the substrate contains:
  - 2 VELO tiles (silicon sensors bump bonded to a row of 3 VeloPix ASICs).
  - 1 GBTx board, which controls 6 VeloPix ASICs directly from the e-ports.

- Due to the highly non uniform radiation, ASICs in the periphery have ten times less occupancy than central ones, using one readout link instead of four. Each module use 20 high speed links come out of VELO module using VELO Gigabit Wireline Transceiver (GWT) serialiser at 5.12 Gbit/s. This serialiser has been specifically designed for VELO in order to reduce the power consumption of VeloPix ASICs.

VeloPix ASIC specifications
Tech: 130 nm CMOS
256×256 pixels; size of 55×55 μm^2
Radiation hardness: 4 MGy
Low power consumption < 1 W/cm^2
Hit peak rate of 900 MHits/s/ASIC
Binary data driven readout at 40 MHz
Maximun output data rate of 20.48 Gbit/s

Table 2: VeloPix ASIC

2.2 Flex tapes

Flex tapes of 56 cm have been produced and tested. First version designed at USC and produced at CERN, were made on 175 µm thick Pyralux AP plus.

Dielectric with traces and gaps of 200 µm. The second version, produced at industry, by reducing traces to 180 µm, improve the whole readout chain impedance match while keeping transmission losses.

2.3 Vacuum feedthrough and opto power board

The Vacuum Feedthrough Board (VFB) is responsible for bringing the electrical connection in and out of the vacuum tank, such as: High speed control and readout signals, analog monitoring signals, high and low voltage power supplies, etc.
The Opto Power Board (OPB) is connected to the VFB outside the vacuum tank. It is responsible for providing the low voltage power supply to the front-end and acting as a link between electrical signals and optical communication with the off-detector electronics.

3. VELO off-detector electronics

The LHCb upgrade uses a common readout board for all off-detector electronics. The board, called PCIe40, is based on the Altera Arria 10 FPGA and the roles of these boards in the experiment (SOL40, TELL40) are determined by its firmware only.
For testing purposes the different functionalities are combined into a single system called MiniDaq.
The first version of MiniDaq has been used to test prototypes of the on-detector electronics.

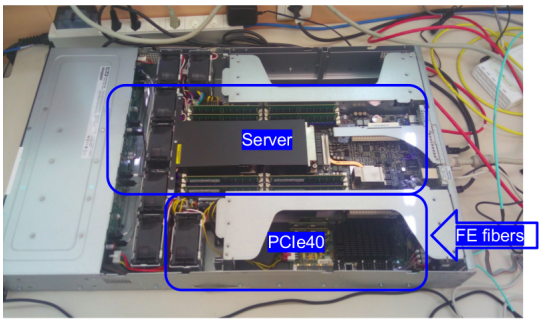

Figure 2: MiniDAQ2

- The SOL40 boards distribute the control signals to all the front-ends chips and keep the whole experiment synchronous. As a single SOL40 provides 48 control links, a total of four SOL40 boards are needed for controlling the 156 links of the whole VELO.
  The LHCb SOL40 common firmware was modified matching with VELO requirements in order to control the front-end VeloPix ASICs directly from the GBTx e-ports.

- The TELL40 boards are responsible for high speed data acquisition with a maximum data rate of 100 Gbit/s, making it possible to read out the complete VELO module with 20 GWT

links. Therefore a total amount of 52 boards will be needed for VELO upgrade.
The LHCb TELL40 firmware was almost completely redesigned in order to comply with the VELO specific requirements, for example. New low level interface that match with the VELO GWT specifications, packet sorting according to its timestamp.

4. VELO upgrade electronics validation

4.1 VeloPix

Two different setups are used to test VELO upgrade electronics. The SPIDR system, is used to characterise the VeloPix ASICs and consist of VeloPix carrier board + Xilinx VC707 evaluation board. This system provides a basic readout without the LHCb specific formatting of the data and already was used to test different ASICs of the TimePix family. The second system is the full LHCb VELO readout system, which is being developed and tested with different prototypes of the system described on section 2 and 3.

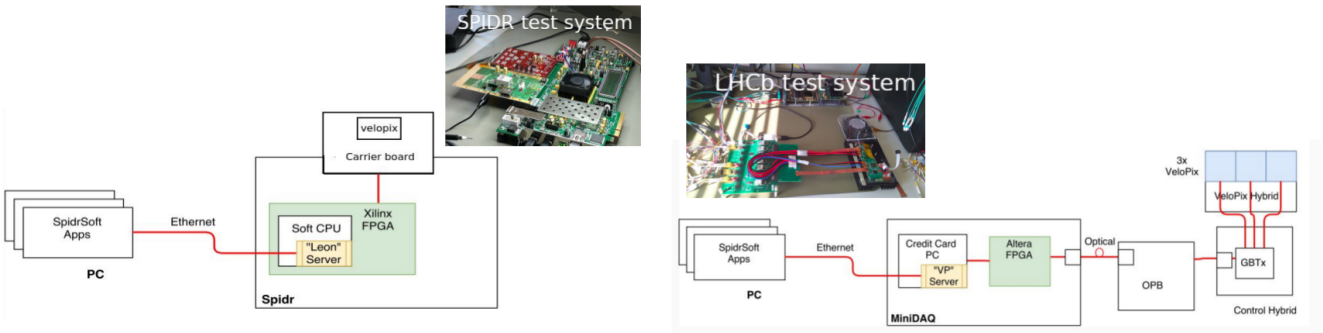

Figure 3: SPIDR vs LHCb test system

A first version of the VeloPix has been produced in July 2016 and carefully tested during the last 12 months, providing input the second version of the VeloPix, which is now under production with the following improvements:

- The digital and analog functionalities have been validated according to specifications. The behaviour of the VeloPix was also tested at temperatures down to -40 °C. An excess of jitter on the GWT serial link recommends a new version of the VeloPix to mitigate transmission errors.

- The chip was successfully operated with Total Ionizing Dose (TID) up to 4 MGy. No change in digital power consumption was observed, nor a drift in analog parameters like thresholds, noise or DAC values.

- Single Event Latch-up (SEL) and Single Event Upsets (SEU) in the line receiver of the reset pin were found at heavy ion beam tests. This behaviour won't allow the ASICs to work on the LHC environment, thus requiring a new version of the VeloPix.

4.2 High speed links

VELO front-end electronics uses two different protocols for the high speed links, CERN standard GBT and VELO specific GWT.

- Front-end GBT links are used for the slow control (ECS) and timing and fast control (TFC) of a hybrid @ 4.8 Gbit/s. In order to allow the electrical signal to travel along the OPB + VFB + 50 cm flex cable, CERN standard GBLD (GigaBit Laser Driver) ASIC is being used as a line driver giving good quality signal at the end of the path. However a passive Continuous Time Linear Equalizer (CTLE) made with discrete components, will be implemented on the receiving end of the links to further improve the quality of the signal.

- The GWT links have been tested with output patterns like Pseudo-Random Binary Sequence (PRBS15, PRBS31) and scrambled data. The observed excess jitter on the clock in the VeloPix ASIC in combination with the frequency dependent attenuation of the flex cables causes the eye diagrams to close, thereby giving rise to a too high Bit Error Rate (BER). By introducing a CTLE circuit, similar to GBT links, the BER can be improved from order 1E-7 to 1E-15.

4.3 Functional verification

Off-detector and on-detector electronic prototypes are currently under test. In order to test the GBT high speed links it was necessary to migrate the slow control communication of SPIDR system to LHCb VELO test system, allowing the validation of the VELO upgrade hardware, SOL40 firmware and test one full sensor tile.
The TELL40 firmware for the data acquisition was successfully simulated and implemented on VELO prototype system FPGA (MiniDAQ1).

5. Summary and Outlook

The on-detector electronics of the VELO upgraded have been successfully validated, and a pre-series of module production started. In parallel, we are working on the data acquisition firmware, with the purpose of getting data from VeloPix ASIC via MiniDAQ. Last but not least, all the off-detector firmware is being migrated from the test FPGA (MiniDAQ1) to final one.

6. Acknowledgements

We gratefully acknowledge the support of the University of Santiago de Compostela, Spanish council of economy and competitiveness and all the people involved on LHCb VELO upgrade.

References

[1] LHCb Collaboration, LHCb Detector Performance, arXiv:1412.6352v2 [hep-ex] 11 Mar 2015

[2] The LHCb Collaboration, LHCb VELO Upgrade Technical Design Report,CERN-LHCC-2013-021 (2013)