PROCEEDINGS OF SCIENCE

A real-time demonstrator for track reconstruction in the CMS L1 Track-Trigger system based on custom Associative Memories and high-performance FPGAs

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A Real-Time demonstrator based on the ATCA Pulsar-IIB custom board and on the Pattern Recognition Mezzanine (PRM) board has been developed as a flexible platform to test and characterize low-latency algorithms for track reconstruction and L1 Trigger generation in future High Energy Physics experiments. The demonstrator has been extensively used to test and characterize the Track-Trigger algorithms and architecture based on the use of the Associative Memory ASICs and of the PRM cards. The flexibility of the demonstrator makes it suitable to explore other solutions fully based on a high-performance FPGA device.

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1. Introduction

The increase of the luminosity to 5×10^{34} cm^{-2} s^{-1} expected in the Large Hadron Collider (LHC) after the upgrade foreseen in 2025 will bring the number of minimum bias interactions per bunch crossing to about 140, on average. In CMS [1], data reduction based on low-latency (<5us) track reconstruction from high-resolution Silicon Tracker information is requested to keep the Level-1 trigger rate below 1MHz. Only data associated with high-Pt tracks (i.e. tracks with energy >3GeV, corresponding to about 3% of the tracks) would be propagated to the Level-1 trigger system.

Different algorithms for track reconstruction have been studied through high-level simulations during the last few years. Hardware implementations have been validated using real-time demonstrators based on state-of-the-art "off-the-shelf" and custom components. We focused on algorithms that use only "hits" that match patterns associated to high-Pt tracks pre-loaded in high-density Associative Memory (AM) custom devices. Track reconstruction algorithms are then implemented in high performance FPGAs and generate the trigger primitives for the Level-1 trigger processor.

We developed a proof-of-concept real-time demonstrator based on the Pattern Recognition Mezzanine (PRM06) board, a custom printed circuit board that houses 12 AM06 ASICs (128K patterns each, for a total of up to 1.5M patterns in each PRM) and a Xilinx Kintex UltraScale FPGA. As host board for the PRMs we used the Pulsar-IIB board, a general purpose ATCA custom board developed at FNAL for the implementation of data acquisition and Level-1 trigger systems in HEP experiments. This board provides an ideal backbone for the development of scalable architectures requiring high bandwidth board-to-board communications.

2. System Architecture

Our demonstrator is based on the assumption that the CMS Silicon Tracker for the High-Luminosity upgrade of the LHC will be segmented in 48 regions (trigger towers) in η-ϕ (pseudo-rapidity and azimuthal angle), 6 in η and 8 in ϕ. An ATCA crate, populated by Pulsar-IIB boards [2], will handle one (in the demonstrator) or two (in the final system) trigger towers. A first $O(10)$ data reduction will be performed in the Tracker modules through "stub" filtering. Only "stubs" - i.e. pairs of hits in the two adjacent sensors associated to high-Pt tracks - will be propagated to the ATCA crates. On average about 100 "stubs" per bunch crossing will be received in each trigger tower from each layer (6 or 7 layers depending on η).

The Pulsar-IIB board is the backbone of our demonstrator. A custom Rear-Transition-Module (RTM) houses the optical transceivers handling the links from/to the detector and the Level-1 trigger processor. Each Pulsar-IIB is connected to all the other boards of the crate through a full mesh high-speed network implemented in the ATCA backplane. This full-mesh connectivity will allow time multiplexing: data associated to different bunch crossings will be distributed to different PRMs, each one processing a single event. A high-performance FPGA (Xilinx Virtex7) handles the data flow from the RTM (40 GTHs) to the two mezzanine boards (12 GTHs) and to the ATCA backplane (28 GTHs). Four FMC connectors allow the insertion of two PRM mezzanine cards.

The PRM board [3] and its architecture are shown in Fig.1. The two FMC connectors carry 6 bidirectional high-speed (8Gbps) serial links. There are also 68 LVDS pairs for configuration (JTAG) and PRM control and monitoring. Power is supplied at 3.3 V and 12 V, with a maximum available power of 150 W. The PRM power management system generates the 1.0V, 1.2V, 1.8V and 2.5V voltages required by the PRM active components (FPGA, AM ASICs and pattern memory containing a copy of the pattern banks of the AM ASICs). The Xilinx UltraScale KU060 FPGA handles the data flow between the host board and the PRM and the handshaking with the AM ASICs and it implements the track reconstruction algorithms.

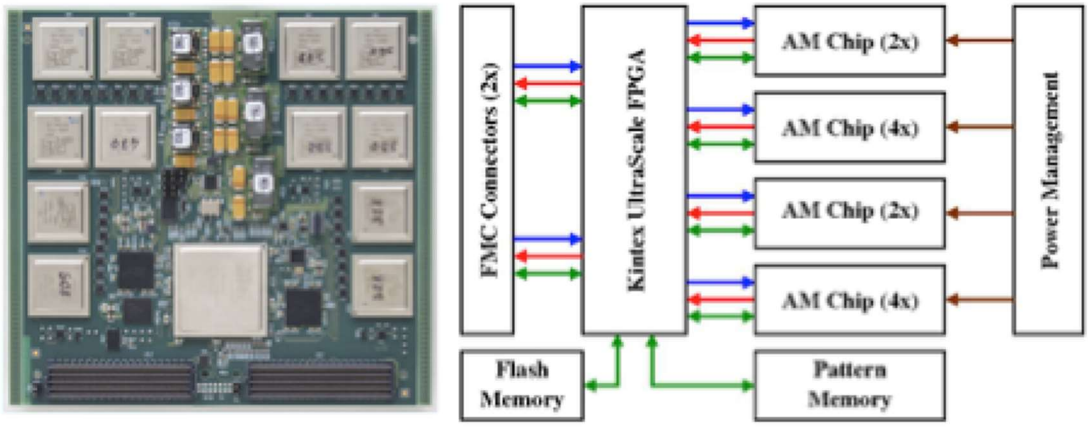

Fig.1: the INFN PRM board (block diagram on the right)

3. Firmware implementation

The architecture of the firmware implemented in the Pulsar-IIB FPGA (Xilinx Virtex7 Xc7vx690tffq1927-2) and the resource utilization are shown in Fig.2.

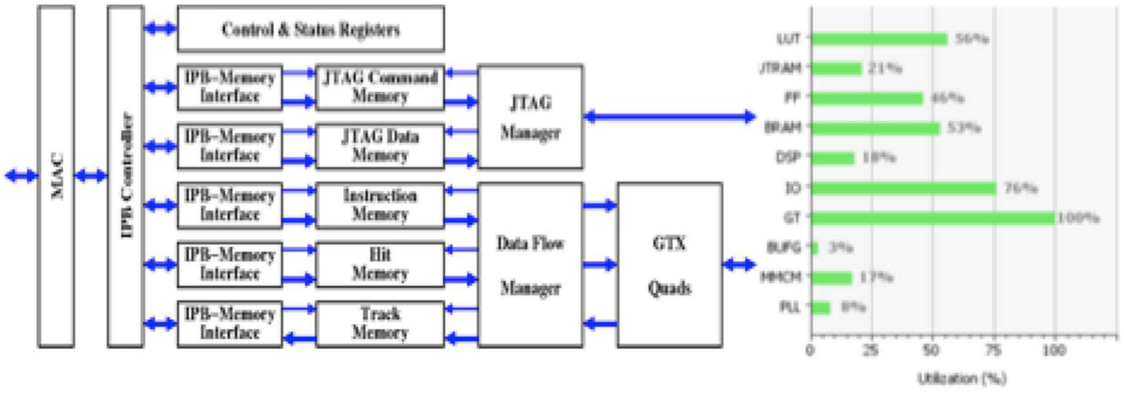

Fig.2: Pulsar II-B Firmware (architecture and FPGA required resources)

An Ethernet interface to/from the ATCA backplane with PHY and MAC embedded in the FPGA handles communication with the host PC. Data transfers to/from all the firmware components (command and data memories, control and status registers) follow the IP-Bus

protocol. The JTAG Manager executes the sequence of JTAG instructions pre-loaded in the JTAG command memory and the patterns stored in the JTAG data memory are loaded via JTAG into the PRM AM chips. The Data Flow Manager (DFM) executes the instructions pre-loaded in the Command Memory (CM). The DFM manages the data transfers to the PRMs from the Stub Data Memory (SDM), pre-loaded with Stubs associated to one or more events (input data), and from the PRMs to the Track Data Memory (TDM) that will be filled with the Track Candidates (output data). This methodology, based on the execution of a set of instructions pre-loaded in the CM and mapped into control signals for all the firmware components, provides a flexible and ready-to-use environment for the validation of our system, but it could be easily modified to test and characterize other options based on different algorithms and FMC-compatible hardware.

The architecture of the firmware implemented in the PRM FPGA (Xilinx UltraScale (Xcku060-ffva1156-1-c)) and the resource utilization are shown in Fig.3. Full resolution data (Stubs) from the host board are mapped into lower resolution data (Super-Strips) that are transmitted to AM ASICs for pattern matching. Stubs are also stored in the Data Organizer (DO), a "smart cache" from where Stubs associated to "hit patterns" in the AM chips will be retrieved.

AM chip output data (Roads) – i.e. the addresses of the "hit patterns" - are used to retrieve from the external Pattern Memory (PM) the corresponding Super-Strips that will be then used to retrieve the corresponding Stubs from the DO.

The Track Candidate Builder (TCB) rejects Stubs outside the projection of a cone generated from data in the three inner layers and finally the Track Fitter (TF) performs linear fits in R-Phi and R-Z planes with a χ^2 cut. Track Parameters are transmitted back to the host board

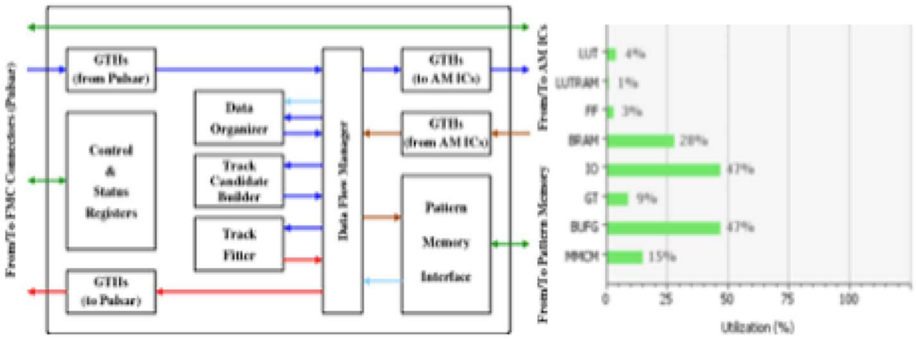

Fig.3: PRM Firmware (architecture and FPGA required resources)

4. Test Results

The final goals of our demonstrator are:

- to evaluate the system performance (latency and efficiency in data filtering),
- to identify possible improvements to match bandwidth and latency constraints,
- to validate the component selection.

In Fig.4 the propagation of the data in the PRM is shown for a t-tbar event with a 140 pile-up. In the considered event the maximum number of stubs per layer was 138, 19 patterns have

been matched and 15 tracks identified, in agreement with the emulation. With the AM ASICs running at the nominal 100MHz clock frequency and with the DO and the TF running at 200MHz and the TCB at 100MHz a processing time of 3.3µs has been measured. For the same event we extrapolated a 1.1 µs processing time with DO, TCB and TF running at their ultimate speeds of 400, 300 and 500 MHz respectively and with AM06 ASICs replaced by the next version of AM08 ASICs (250 MHz).

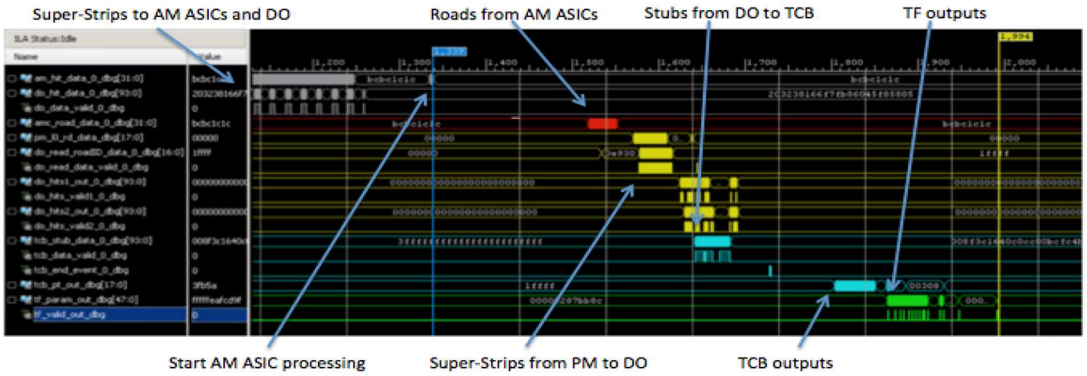

Fig.4: data flow in the PRM based demonstrator

5. Conclusions

A real-time processor for the track finding in the CMS Level-1 trigger system that combines Associative Memory and high-performance FPGA features has been developed. Track reconstruction algorithms and prototypes of the PRM boards housing FPGA and custom Associative Memories devices have been fully validated in dedicated test benches in 2015 and 2016. Final validation and characterization have been performed in 2017 on the demonstrator here presented, based on PRM boards and on the general-purpose Pulsar-IIB ATCA board. The architecture and behavior of the demonstrator make it suitable to explore other solutions fully based on high-performance FPGA devices. The entire Software/Firmware platform is available to hardware and firmware developers interested in having a flexible and ready-to-use environment for the validation of algorithms or hardware solutions.

References

[1]J. Butler et al, "*Technical Proposal for the Phase-II Upgrade of the CMS Detector"*, CERN-LHCC-2015-010

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[3]C. Gentsos et al., "*Track Finding Mezzanine for Level-1 triggering in HL-LHC experiments*", Proceedings of the 6th International Conference on Modern Circuits and Systems Technologies (MOCAST), Thessaloniki, Greece, May 4-6, 2017