PROCEEDINGS OF SCIENCE

Development of the new Trigger Processor Board for the ATLAS Level-1 Endcap Muon Trigger for Run-3

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The instantaneous luminosity of the LHC will be increased by up to a factor of three with respect to the original design value at Run-3 (starting 2021). The ATLAS Level-1 end-cap muon trigger in LHC Run-3 will identify muons by combining data from the Thin-Gap Chamber detector (TGC) and the New Small Wheel (NSW), which is a new detector and will be able to operate in a high background hit rate at Run-3, to suppress the Level-1 trigger rate. In order to handle data from both TGC and NSW, a new trigger processor board has been developed. The board has a modern FPGA to make use of Multi-Gigabit transceiver technology. The readout system for trigger data has also been designed with TCP/IP instead of a dedicated ASIC. This letter presents the electronics and its firmware of the ATLAS Level-1 end-cap muon trigger processor board for LHC Run-3.

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1. Introduction

The instantaneous luminosity of the LHC will be increased by up to a factor of three with respect to the original design value at Run-3 (starting 2021). The ATLAS trigger and data-acquisition system is based on two levels of event selection. The Level-1 trigger is based on hardware and High Level Trigger is processed by software. The ATLAS end-cap muon system needs to be upgraded to keep the trigger rate acceptable at Run-3.

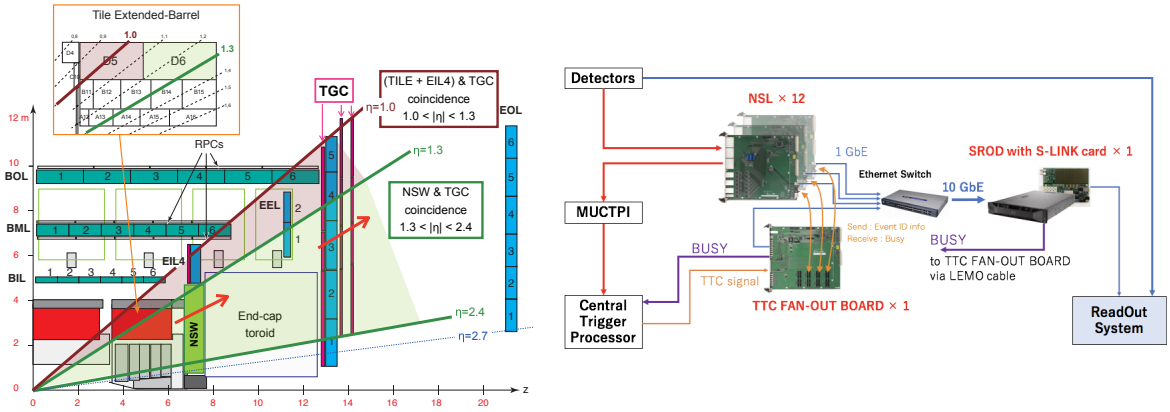

Figure 1: The schematic view of the ATLAS muon spectrometer with the New Small-Wheel [2] (left) and brief diagram of the new read-out scheme for the end-cap muon system (right). Red line shows the trigger data path and blue line shows the readout path.

Figure 1 (left) shows the schematic view of the ATLAS muon system. The TGC Small Wheel and the CSC [1] located between the end-cap calorimeter and the end-cap toroidal magnet will be replaced by the New Small Wheel (NSW) [3], which consists of sTGC and MicroMegas detectors, to reduce the trigger rate by improving the muon tracking performance and the rejection of fake muons by incorporating track-vector information from the NSW [4]. In order to form the Level-1 accept signal in the end-cap muon trigger system using the NSW information and the TGC Big Wheel (TGC-BW), the new trigger processor board (New Sector Logic ; NSL) has been developed. The readout scheme in Fig. 1 (right) is also upgraded and composed of the NSL, TTC FAN-OUT BOARD and Software-based ReadOut Driver (SROD).

2. Development of the new trigger data readout scheme for Run-3

2.1 New Sector Logic (NSL)

The NSL calculates the muon p_{T}, and sends the p_{T} value and Region of Interest (ROI) information to the MUCTPI [5]. A picture of the NSL is shown in Fig. 2 (left). The data from the TGC-BW is received by 14 G-Link optical receivers, and the NSW track-segment information is received by GTX optical transceiver [6]. The main functions of the NSL are implemented in the FPGA, and the firmware diagram is shown in Fig. 2 (right). First, a muon p_{T} is calculated by taking a coincidence using input data from the TGC-BW wires (R) and strips (ϕ). Next, an additional coincidence between the TGC-BW and the NSW is taken to eliminate fake muons and to improve the p_{T} determination by using the coordinate and vector information from the NSW.

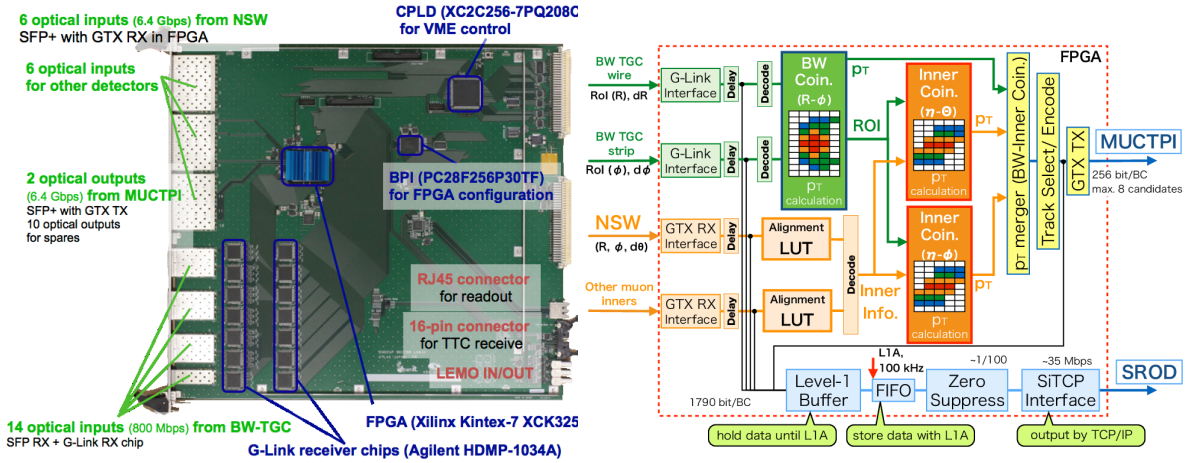

Figure 2: A picture of the NSL (left) and its firmware diagram (right).

2.2 TTC FAN-OUT BOARD

TTC FAN-OUT BOARD has two roles. One function is to propagate timing, trigger and control (TTC) signals [7] to each NSL via flat copper cable and send the event ID to SROD at a maximum rate of 100 kHz. The other is to receive busy signals from each NSL and SROD, taking logical sum of received busies. A picture of the TTC FAN-OUT BOARD is shown in Fig. 3 (left), and the firmware diagram of the TTC FAN-OUT BOARD is shown in Fig. 3 (right).

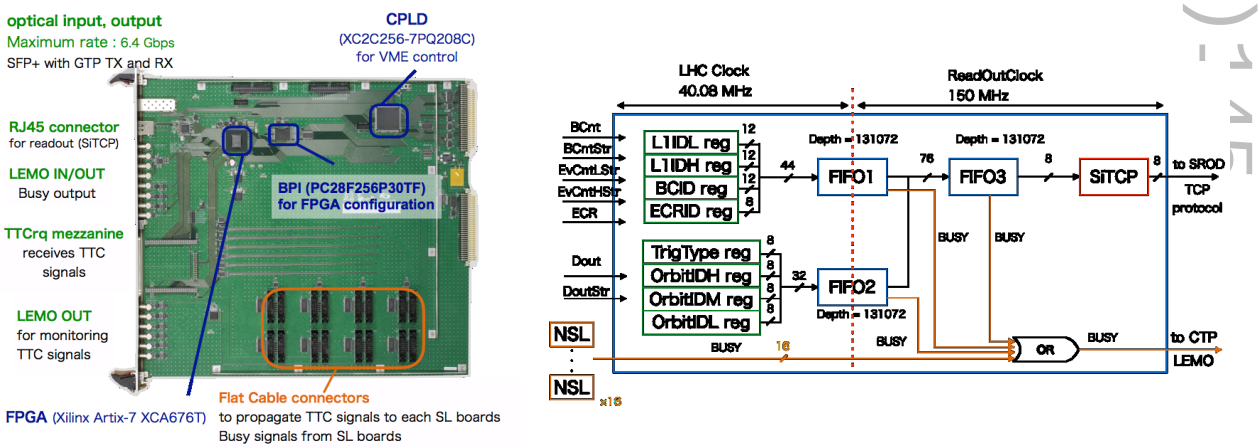

Figure 3: A picture of the TTC FAN-OUT BOARD (left) and its firmware diagram (right).

2.3 Software-based ReadOut Driver (SROD)

The SROD is implemented by multi process on commercial PC. SROD PC contains NSL/TTC Collector, Ring Buffers, Run Control Driver (RCD) and Event Builder. NSL/TTC Collector reads data from the NSL/TTC FAN-OUT boards. The Ring Buffer absorbs the timing variation in receipt of data. The Event Builder reads data from the Ring Buffer and builds the ROD event fragments.

The RCD synchronizes each process state with the ATLAS detectors. Figure 4 shows a picture of the PCIe S-LINK card [8]. The S-LINK is a CERN specification for FIFO-like data-link which can be used to connect front-end to read-out in a data flow environment. The PCIe S-LINK card is mounted on the SROD PC and sends data to the ATLAS readout system [9]. This card also has LEMO connectors to send the busy signal from the SROD by open-drain to the TTC FAN-OUT BOARD.

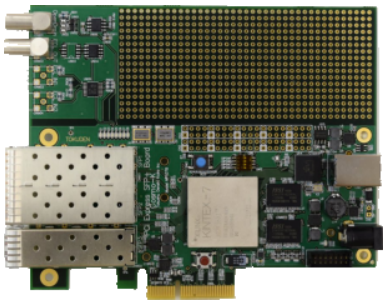

Figure 4: A picture of the S-LINK card.

3. Conclusion

The ATLAS Level-1 end-cap muon trigger in LHC Run-3 will identify muons by combining data from the TGC and the NSW. In order to handle data from both TGC and NSW, the new trigger processor board, NSL has been developed. The new readout system has also been constructed with TCP/IP instead of a dedicated ASIC.

References

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