

Construction and Commissioning of the Phase 1 Upgrade of the CMS Pixel Detector

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The Phase 1 upgrade of the CMS pixel detector, installed by the CMS collaboration during the recent extended end-of-year technical stop, is built out of four barrel layers (BPIX) and three forward disks in each endcap (FPIX). It comprises a total of 124M pixel channels, in 1856 modules and it is designed to withstand instantaneous luminosities of up to $2 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$ with increased detector acceptance and additional redundancy for the tracking, while at the same time reducing the material budget.

These goals are achieved using a new readout chip and modified powering and readout schemes, one additional tracking layer both in the barrel and in the disks, and new detector supports including a CO₂ based evaporative cooling system.

Different parts of the detector have been assembled over the last year and later brought to CERN for installation inside the CMS tracker. At various stages during the assembly tests have been performed to ensure that the readout and power electronics, and the cooling system meet the design specifications. After tests of the individual components, system tests have been performed before the installation inside CMS.

This contribution will review the design and technological choices of the Phase 1 detector, with a focus on the challenges and difficulties encountered, and present results from system tests and from the final commissioning of the detector in-situ using the central CMS DAQ system.

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1. Introduction

During the extended year end technical stop 2016/2017 the CMS Collaboration [1] replaced its pixel detector with an upgraded Phase 1 pixel detector [2]. The readout chip (ROC) in the original pixel detector was not suited for operation at an instantaneous luminosity of $2 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$. Luminosities of $1.5 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$ were already seen in 2016 and a dynamic inefficiency was observed. These dynamic inefficiencies can be seen in Figure 1 left for 2016 data and with the instantaneous luminosity expected to rise in 2017 and 2018, the dynamic inefficiency would have increased effecting physics performance, thus the CMS pixel detector was replaced. This Phase 1 pixel detector will operate in CMS until Long Shutdown 3 or the start of the High Luminosity LHC.

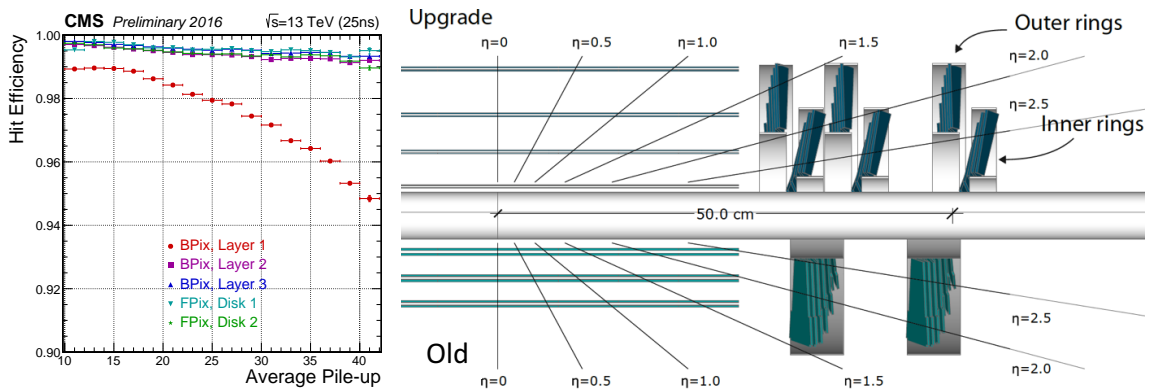


Figure 1: Hit efficiency (left) with respect to average pile-up, number of simultaneous interactions, for 2016 data. Layer 1, the layer closest to the interaction point, experiences the highest particle fluencies and therefore exhibits the highest dynamic inefficiency. The right diagram shows the detector layout of the original pixel detector (bottom) and the upgraded detector (top) [2].

The old versus the new pixel detector layout can be seen in Figure 1 right. The upgraded pixel detector has one more sensitive layer in both the barrel (BPIX) and forward (FPIX) regions than the original CMS pixel detector giving four-hit coverage up to a pseudorapidity, η , of $|\eta| < 2.5$. The layer closest to the interaction point was moved in with respect to the original CMS pixel detector and therefore the beam pipe had to be replaced. This was done during Long Shutdown 1. The layer closest to the interaction point, layer 1, sits at a radius of 3 cm from the interaction point.

2. Module Production

The pixel modules share the overall structure of the pixel modules from the original CMS detector. They consist of active silicon sensors that are bump bonded to 16 ROCs. These ROCs then communicate with the Token Bit Manager (TBM) via the High Density Interconnect (HDI). The HDI is connected to the ROC via a series of wire bonds. The silicon sensors are n+ in n sensors with a pitch of $100 \times 150 \mu\text{m}^2$ like in the previous CMS pixel detector, however the TBM and ROC were changed to cope with the higher particle rates.

The TBM [3] is an ASIC that merges data from the ROCs with 320 Mbps readout rate. There are three versions of the TBM used in the Phase 1 CMS pixel detector: as single data stream for BPIX layers 3-4 and all disks of FPIX, two data streams for BPIX layer 2, and four data streams for BPIX layer 1. There are actually two TBMs on layer 1 modules to cope with the high particles rates expected.

To cope with the high particle rates, the ROCs on layer 1 are also different from the other modules in the Phase 1 CMS pixel detector. The layer 1 ROC is called PROC600, indicating it was designed to maintain high efficiency even with hit rates in excess of 600 MHz per cm^2 . This ROC builds clusters of 4 pixels inside the double column architecture before transmitting the cluster information. This chip was developed specifically for this upgrade and was demonstrated to be radiation hard in test beam. The PROC600 has 339 transistors per pixel as compared to the ROC for all other modules which only has 268.

BPIX layers 2-4 and all of FPIX use the PSI46digV2.1respin [4] ROC in their modules. This CMOS ASIC is based on the ROC from the original CMS pixel detector where a double column architecture was used. A token travels up an 80 pixel column and then down another creating a double column. Each double column has 80 data buffer cells and 24 timestamp buffer cells. While the buffer size was increased and the functionality was moved from analog to digital, the overall architecture and 250 nm feature size are the same as the original CMS pixel ROC PSI46. This upgraded chip performs better because it has a lower noise threshold of 1800 e- compared to the original 3200 e- seen in PSI46.

Pixel modules were assembled in 2016 in two assembly sites in the USA for FPIX and 6 sites in Europe for BPIX. While the modules themselves were very similar with 16 ROCs bump bonded to silicon with HDI on top connected with wire bonds, the BPIX and FPIX modules used very different assembly methods. BPIX modules were assembled using precision made jigs that had adjustable micro metric screws for fine alignment. FPIX modules were assembled using Aerotech robotic gantry systems. All modules were graded with a shared set of qualification criteria so that modules with too many dead pixels were not used for installation in the upgraded CMS pixel detector.

A common suite of tests were used to qualify the modules after assembly including testing the functionality of ROC, TBM, and pixel response. These tests were performed in a humidity and temperature controlled cold box. Results from module testing were used as a starting point for commissioning. X-rays were also used for the pulse-height calibration and high rate test.

3. Detector Infrastructure

A large constraint of the Phase 1 pixel project was that only existing power cables would be available to power 1.9 more channels than in the original CMS pixel detector. This was achieved by developing DC-DC converters that convert high-voltage low-current to low-voltage high-current inside the service cylinder of the CMS pixel detector. Specifically these converters convert 11V input voltage to 2.4V and 3.3V-3.5V lines used by the pixel modules. A total of 1184 converters were needed for this detector requiring an intense testing campaign before installation. DC-DC converters were thermal cycled 10 times from -20°C to 28°C and classified according to their out-

put voltages. Only the best performing DC-DC converters were installed in the new pixel detector. The DC-DC converters also serve as preheaters for the CO₂ cooling lines.

For the upgrade CMS replaced C₆F₁₄ coolant with biphasic CO₂ cooling [5]. This required smaller capillaries and contributed to reducing the material budget. Figure 2 left shows a 1.6 mm tube embedded in a FPIX half disk, while Figure 2 right shows cooling lines running between BPIX ladders. Cooling lines were pressure tested to 150 bar and leak tested at 100 bar. The operating pressure for the Phase 1 upgrade CMS pixel cooling system is 20-30 bar.



Figure 2: CO₂ cooling tube embedded in FPIX disk (left). Cooling lines between the BPIX ladder (right) [5].

Despite an additional tracking layer in both the barrel and forward regions the overall material budget for the CMS pixel detector actually decreased. This was achieved in several ways. The change from C₆F₁₄ to CO₂ cooling allowed for thinner capillaries, reducing the amount of material in the cooling system. Lighter mechanical supports were used. In the FPIX system the original CMS pixel detector used metal support frames, while the Phase 1 upgrade CMS pixel detector uses carbon fiber and thermal pyrolytic graphite. The material budget in the active detector area was also reduced by simply moving electronics forward along the beam pipe. This was achieved by designing nested service cylinders that moved DC-DC converters, port cards, laser drivers, and other supply and control electronics away from the pixel modules themselves and forward of the active detector area.

4. DAQ

The data acquisition system (DAQ) for the CMS pixel detector was updated to μ TCA from the outdated VME system. VME front-end boards were replaced by 108 Front End Drivers (FED) for detector readout and 16 + 3 Front End Controllers for detector control. These boards sit off the detector in the underground service cavern and therefore do not need to be radiation hard nor be able to withstand high magnetic fields. μ TCA is the new CMS-wide standard DAQ system based on generic AMC cards with a Kintech7 FPGA and 4GB DDR3 RAM. The detector front end was replaced with emulated data to test the FED firmware and validate data throughput to CMS central DAQ before the detector was installed. The system was commissioned as much as possible before installation on test stands at institutes and a test stand at the main site at CERN. Much development, however, happened after the μ TCAs were connected to a FPIX half cylinder starting September in 2016.

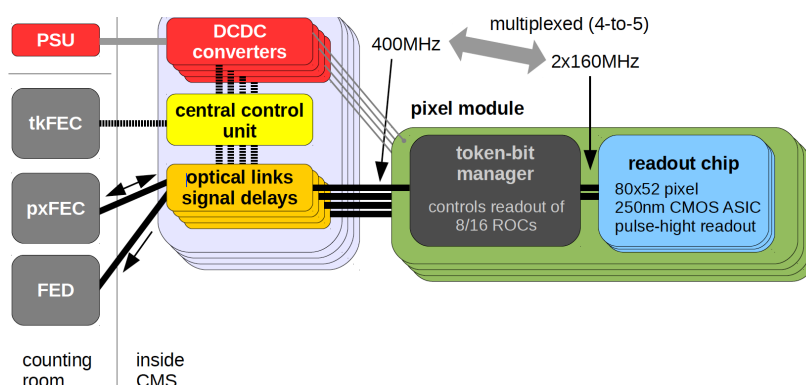


Figure 3: A block diagram of some of the connections that needed to be verified and calibrated before the upgraded pixel detector was ready to take data [6].

5. Detector Checkout and Commissioning

Detector checkout was achieved through several steps [6]. Figure 3 shows some of the connections that needed to be checked out and calibrated before the Phase 1 pixel detector was ready to take data, even cosmic data. First optical connections were tested and optimized. This involved cleaning fibers to ensure the light quality was high and varying light levels to ensure connections were correct. Then supply signals were adjusted by adjusting signal delays. Then external 400 MHz and internal 160 MHz TBM phases were found so that complete data words can be decoded in the FED. The last step of detector check out was to inject and readout test hits on individual pixels. This check out procedure was done for FPIX when the half cylinders arrived at the CERN main campus from the USA and then was repeated above ground at point 5 before the half cylinders were installed in the heart of the CMS detector. The BPIX underwent check out above ground at point 5 before installation. This check out procedure was repeated one final time before the start of the cosmic run.

There was a short commissioning period with cosmic muons before collision data taking started. During this time reconstructed tracks could be seen in the new pixel detector. Also a few non working areas of the detector were identified. Larger areas of missing hits were due to power group or readout group issues. Some modules were not giving good hits due to a variety of problems including: TBM problem, cable problem, etc. There were also a few ROCs that were not recording good hits. This is expected in a system with millions of channels, so these few failures do not affect the physics performance. Over 95% of the channels give good physics data.

6. Conclusions

The new Phase 1 upgrade pixel detector was successfully installed in CMS in early 2017. The commissioning effort was just wrapping up when this talk was given in July 2017 and is now done. Around 95% of detector channels are working without problem. This detector will outperform the original CMS pixel detector and will yield high quality data until Long Shutdown 3.

References

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