PROCEEDINGS OF SCIENCE

The ALICE ITS upgrade

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A major upgrade of the Inner Tracking System (ITS) of the ALICE experiment at LHC is currently under preparation with the aim of exploiting the increased Pb-Pb luminosity expected during Run 3 and Run 4 after 2020, which will enable to make a detailed study of the properties of the Quark-Gluon Plasma. The new ITS, which will be installed during the Long Shutdown 2 (2019-2020), will increase the readout rate capability by more than two orders of magnitude while, at the same time, improving the tracking capability and the impact parameter resolution, especially at low transverse momentum.
The new ultra-light tracker will be constructed with Monolithic Active Pixel Sensors to instrument the ~10 m^2 ITS active surface, arranged on seven layers, with the inner layer as close as 23 mm from the interaction point.
The CMOS chip (ALPIDE) which will equip the ITS is built in the TowerJazz 180 nm - CMOS imaging sensor process and has been custom designed to fulfil the stringent requirements of the new tracker.
The chip R&D phase finished in 2016 with the development of a chip whose performances fulfil and often exceed the project requirements. The start of production of ALPIDE in December 2016 marked the beginning of the production phase of the ITS upgrade.

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1. Introduction

The main objective of the ALICE experimental program for Run 3 and 4, after Long Shutdown 2 (LS2) in 2019-20, is a detailed exploration of the properties of the Quark-Gluon Plasma via high precision measurements of rare probes in pp, p-Pb and Pb-Pb collisions [1]. In order to be able to measure a high statistics sample of short lived systems such as heavy flavor hadrons, quarkonia and low mass dileptons, over a wide range of transverse momenta, it will be necessary to enhance the tracking and readout rate capabilities of the present detector and in particular of the Inner Tracking System (ITS) [2]. During LS2 several sub-detectors will we upgraded and the present ITS will be replaced with a new detector exclusively equipped with Monolithic Active Pixel Sensors (MAPS).

2. The upgrade of the Inner Tracking System

The present ITS [3] is composed of two layers of silicon hybrid pixel sensors, two layers of silicon drift sensors and two layers of silicon micro-strip sensors. It has fully met the requirements of the experiment in Runs 1 and 2 but it will not be able to cope with the future Pb-Pb interaction rate of 50 kHz and its pointing resolution does not permit the efficient reconstruction of secondary vertices characteristic of heavy flavor decays, particularly at low transverse momenta (p_T < 1 GeV/c).

To fulfill the stringent requirements of the ITS upgrade, a new layout was designed and optimized [2]. The key improvements are a large reduction of the material budget (0.3% X_0 per layer for the inner layers, 1% X_0 for the outer layers) with a new layout with the addition of a new layer, the first layer closer to the interaction point and the use of pixel sensors of about 30x30 μm^2 pixel size. The new layout will allow to strongly improve the efficiency at low transverse momenta (~70% at p_T = 100 MeV/c) as well as the impact parameter resolution, as can be seen in figure 1.

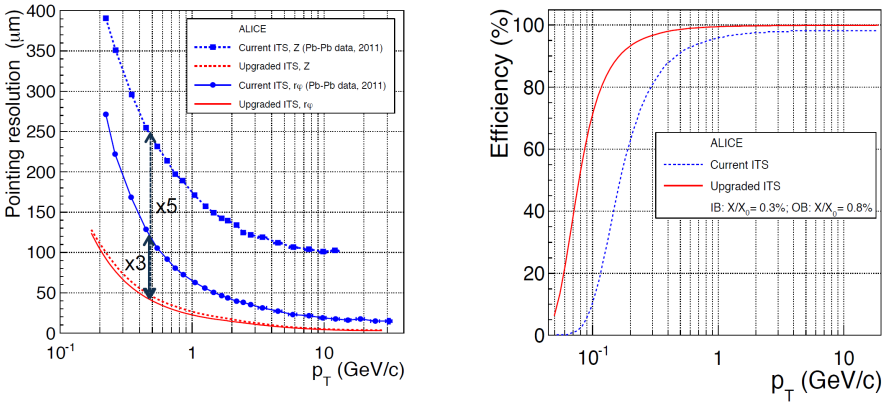

Figure 1: On the left the pointing resolution as a function of p_T. On the right the efficiency as a function of p_T. The blue curves and dots refer to the present ITS, while the red curves are the Monte Carlo predictions for the new ITS.

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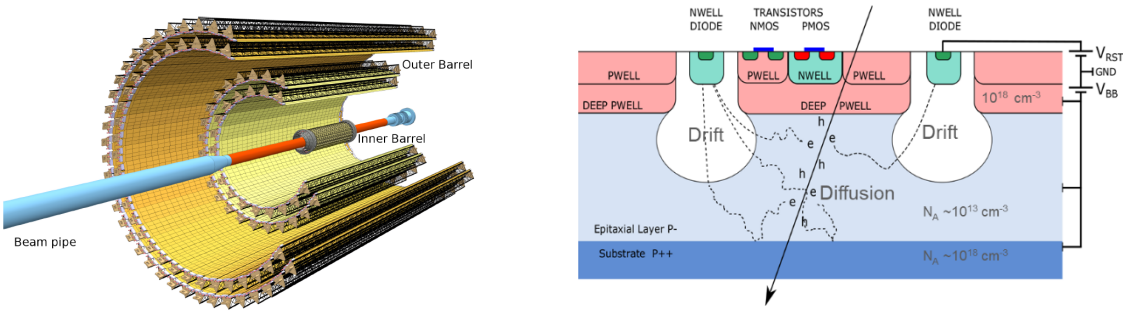

Figure 2: Left: Schematic layout of the upgraded ITS. Right: Schematic view of a transverse section of the ALPIDE chip.

The layout of the new ITS is illustrated in figure 2 (left). It is composed of 7 layers, consisting of 3 inner layers, referred to as Inner Barrel (IB), and 4 outer layers, referred to as Outer Barrel (OB), with the outermost layer at a radius of 405 mm.

Together with the low sensors thickness (50 μm for the IB and 100 μm for the OB), the material budget was kept low by the use of carbon fiber structures (staves) to support the chips, mounted on low mass polyimide Flexible Printed Circuits of different dimensions depending on the layer, and light water cooling pipes integrated in the structures. The staves, of a minimum length of 27 cm for the inner layers and 148 cm for the outer layers, will be equipped with ~1.2 billion custom designed binary readout MAPS sensors to cover an area of ~10 m^2.

More details on the ITS characteristics and the chip R&D can be found in [4-6].

2.1 The pixel sensor

The demanding design requirements discussed above together with those of a low power consumption (<100 mWcm^{-2}) and integration time (<30 μs), required the development of a custom designed sensor chip, which involved a long R&D phase with the production of several prototype chips.

ALPIDE, the MAPS chip developed for this purpose, is fabricated in the 180 nm CMOS imaging sensor TowerJazz process [7], which provides a high resistivity (>1 kΩ cm) p-type epitaxial layer on a p-type silicon wafer and deep p-wells, allowing the implementation of PMOS transistors at the pixel level. This permitted the design of front-end circuitry with very low power consumption (<40 mW/cm^2), an integration time of ~2 μs and a novel readout approach, faster than a traditional rolling shutter.

The high resistivity epitaxial layer provides an increased depleted volume at the collection diode, resulting in an efficient collection of the charge released by the incoming radiation. It is also possible to apply a reverse bias to further increase the depletion volume and improve its radiation tolerance. In figure 2 (right) a schematic cross section of the chip is shown.

The chip measures 15 x 30 mm^2 and contains half million 27 x 29 μm^2 pixels, arranged in 512 rows and 1024 columns. The sensor provides in-pixel amplification, discrimination and

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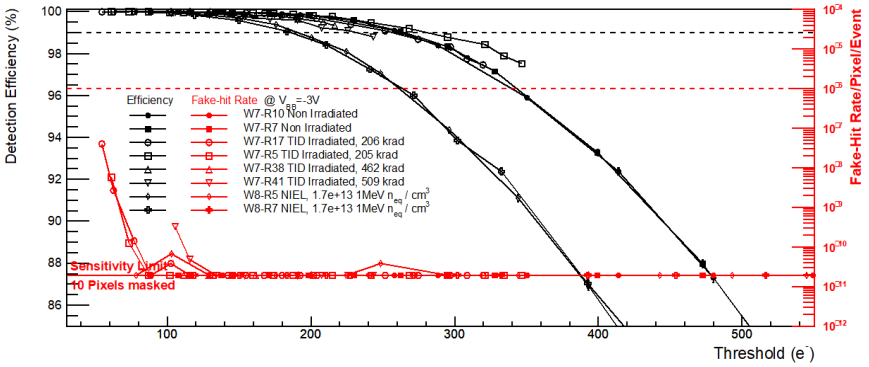

Figure 3: Detection efficiency (left axis) and fake hit rate (right axis) vs. threshold of ALPIDE chips irradiated with different NIEL and TID doses. The dotted lines represent the project requirements. The 10 noisiest pixels were masked. A -3V reverse bias was applied during the measurements.

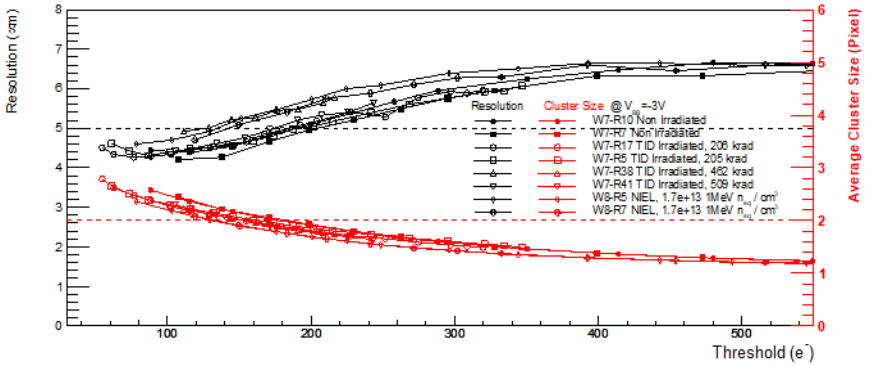

Figure 4: Resolution (left axis) and average cluster size (right axis) vs. threshold for ALPIDE chips irradiated with different NIEL and TID doses. The dotted lines represent the project requirements. A -3V reverse bias was applied during the measurements.

buffering, which allows a zero suppressed asynchronous readout. The most relevant features of ALPIDE are a spatial resolution of ~5 μm, an efficiency better than 99% and a fake hit rate $<10^{-10}$ hits/pixel/event, 4 orders of magnitude lower than required.

Figures 3 and 4 show the results of measurements performed with a 6 GeV/c pion beam as a function of the applied threshold on chips irradiated at different doses. It can be observed that the required performance can be achieved in a rather large operation interval even in presence of a ionizing dose of 500 krad and a NIEL up to 1.7 x 10^{13} 1 MeV n_{eq} / cm^2 (10 times the total dose expected in 10 years of operation).

The use of a high speed serial link (1.2 Gbit/s for the Inner Barrel) for the direct connection of the chip to the external readout electronics, located outside the sensitive volume, will make it possible to achieve the required read out rate (100 kHz in Pb-Pb collisions).

3. Summary

The ALICE Collaboration is preparing a major upgrade of the apparatus with the aim of extending the physics reach of the detector, which will be capable of performing high statistics

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measurements of heavy flavor particles and other rare probes. This will allow ALICE to fully exploit the increased luminosity of LHC in Runs 3 and 4 after 2020.

Crucial to achieving this aim is the new ITS, an ultra-light, low power, rad-tolerant tracker equipped with ALPIDE, a MAPS chip produced in the 180 nm CMOS Imaging TowerJazz process, arranged in 7 layers and covering an active area of approximately 10 m^2 making ALICE the first LHC experiment implementing MAPS technology on a large scale.

The chip R&D phase finished at the end of 2016 with the start of production of ALPIDE, whose performances meet or even exceed the design requirements of the ITS upgrade. The excellent single chip performances were confirmed by fully equipped staves in realistic operational conditions in Pb-Pb collisions at SPS.

References

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