PROCEEDINGS OF SCIENCE

Challenges of front-end and triggering electronics for High Granularity Calorimetry

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A high granularity calorimeter is presently being designed by the CMS collaboration to replace the existing endcap detectors. It must be able to cope with the very high collision rates, imposing the development of novel filtering and triggering strategies, as well as with the harsh radiation environment of the high-luminosity LHC. In this paper we present an overview of the full electronics architecture and the performance of prototype components and algorithms.

EPS-HEP2017, European Physical Society conference on High Energy Physics
5-12 July 2017
Venice, Italy

[1]Speaker

PoS(EPS-HEP2017)514

1. Introduction

The Large Hadron Collider (LHC) has collected about 30 fb^{-1} of proton-proton collisions at $\sqrt{s}$ = 7 and 8 TeV with the most significant result the discovery of the Higgs boson. It is currently running at a centre-of-mass energy of $\sqrt{s}$ = 13 TeV with the physics program consisting of detailed studies of the Higgs boson and standard model (SM) processes as well as searches for physics beyond the SM. Around 70 fb^{-1} have been accumulated at this energy and the LHC plans to increase this to about 300 fb^{-1} by the end of Run 3 (2023). After the third long shutdown the high-luminosity LHC (HL-LHC) is scheduled to start in 2026, planning to accumulate about 3000 fb^{-1} by the mid 2030s. HL-LHC will operate with very high event pileup, and key to achieving its important physics goals is the triggering and reconstruction of physics processes initiated by vector boson fusion, involving for example narrow or merged jets in the forward region.

The existing forward calorimeters in the CMS (Compact Muon Solenoid) detector were designed for an integrated luminosity of 500 fb^{-1} and will have to be replaced by a new generation of calorimenters built with radiation hard technologies [1]. The CMS collaboration will build a high granularity calorimeter (HGCAL) as part of its HL-LHC upgrade program.

The HGCAL consists of electromagnetic (CE-E) and hadronic (CE-H) parts with very high transverse and longitudinal segmentation, which will enable efficient particle-flow calorimetry and help in triggering, pileup rejection and particle identification. CE-E and a part of CE-H will be based on hexagonal silicon sensors with a cell sizes of $O(0.5–1\ cm^2)$, with the remainder of CE-H based on highly-segmented plastic scintillators with silicon photomultiplier (SiPM) readout. The high-precision timing capabilities of the silicon sensors will be used as an extra dimension in event reconstruction, while its intrinsic high radiation tolerance will meet the requirement for HGCAL running beyond the HL-LHC targeted luminosities.

More information about HGCAL general properties is given in these proceedings [2]. In this paper we present an overview of the full electronics architecture and the performance of prototype components and algorithms.

2. Front-end electronics requirements and architecture

The front-end (FE) electronics has four main roles: measurement and digitization of the charge deposited in the silicon sensors or generated in the SiPMs, high precision measurement of the time of arrival (ToA) of the pulses, computation of digital sums of neighbouring cells for trigger primitive generation (TPG), and transmission of digitized data to the back-end (BE) electronics.

The same FE electronics will be used for the readout of the silicon sensors and of the SiPMs. Since the silicon sensors are more demanding, they are driving the main requirements on the performance of the FE electronics: *low noise and large dynamic range* (from ~ 0.2 fC to 10 pC, equivalent to 16 bits, with the electronic noise ≤ 2000 e^-); non-*linearity better than 1%* over the full range; *timing precision better than 50 ps* for pulses above ≈ 12 fC; *fast shaping time* (peaking-time ≤ 20 ns) to minimize the out-of-time pileup; *on-detector digitization and data processing*; *data buffering* to accommodate the 12.5 μs latency of the L1 trigger; *high-speed readout links* to interface with the 10 Gb/s low-power GBT (LpGBT) [3] serialiser; *low*

power budget (≤ 20 mW per channel for the FE electronics); *high radiation resistance* (≥ 1.5 MGy and 1×10^{16} n_{eq}/cm^2).

The basic electronics architecture is shown in Figure 1. The central part of the architecture is the front-end ASIC, named HGCROC, which measures the charge and the time of arrival of the signals from the silicon sensors or the SiPMs, at 40 MHz frequency. It consists of 78 channels and is designed in a 130 nm technology. Its total power consumption is estimated to be ≈ 14 mW per channel.

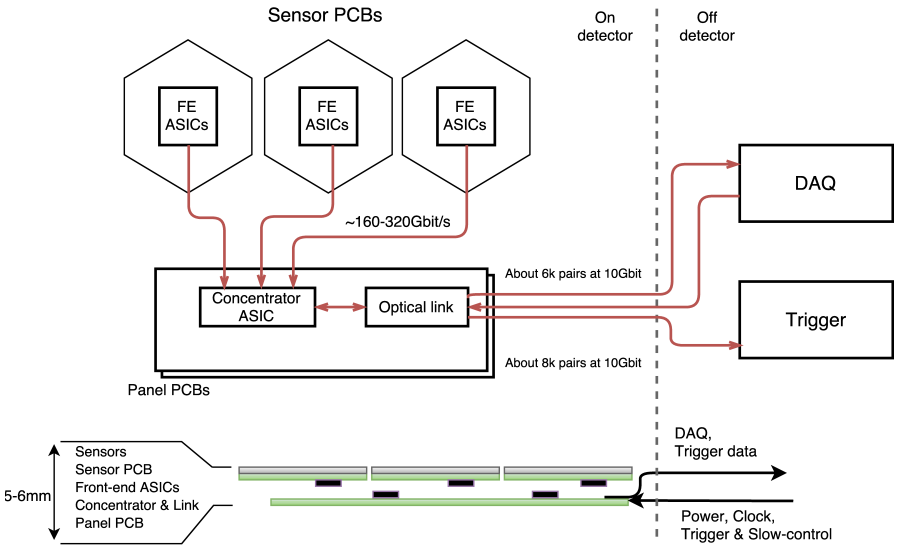

Figure 1: The front-end architecture and motherboards layout [4].

The charge measurement (for silicon sensors) is performed with a 10-bit SAR ADC for charges up to 100-150 fC and by using the time-over-threshold (ToT) technique for charges above ~ 50 fC with a 12-bit TDC. The ToT dynamic range extends the measurement up to 10 pC. The ToA is measured with a 10-bit TDC (< 25 ps step LSB and 25 ns full range). After alignment, the ADC, ToT and ToA data are stored at 40 MHz in a 512-column memory, waiting for a potential L1 trigger accept. ADC and ToT data are recombined, linearised and calibrated to provide a single charge measurement which is used to build trigger sums. Sums of 4 or 9 adjacent channels (depending on the sensor granularity) are formed and the result is compressed with an 8-bit format. Both data and trigger sums are transmitted via 1.28 Gb/s electrical links to the next level of the FE electronics. For the readout of the SiPMs a version of the HGCROC, including a capacitive charge divider, will be produced. HGCROC is based on the SKIROC2 chip [5] for the CALICE collaboration [6]. A development version named SKIROC2_CMS, optimized for the CMS testbeam, shows encouraging results [7].

The next level of the FE electronics is located on separate motherboards serving from 1 to 6 modules, depending on the occupancy of the sensors. The motherboards distribute power to the modules, receive and distribute the fast control and configuration signals, as well as data and control information to the DAQ modules, via bidirectional optical links. This latter uses generic HL-LHC developments: the LpGBT chipset [3] coupled to a Versatile Link [8]. For the trigger path, the concentrator ASIC receives up to sixty-four 1.28 Gb/s electrical links from the

HGCROCs, then selects the trigger sums of interest, aggregates and formats their data and stores them in a FIFO buffer with a length of 12 bunch crossings. Within a defined maximum latency these data are sent to the BE trigger electronics located in the service cavern, using separate optical links at 10 Gb/s. All the ASICs are developed in a radiation-tolerant technology, for doses higher than 2 MGy.

3. Trigger primitive generation (TPG)

The TPG output for each endcap will be a list of three-dimensional (3D) clusters reconstructed from the trigger cells, and a list of η, φ "towers" made from the HGCROC sums. As the input data for a given bunch crossing will arrive to the TPG up to 1.5 μs later, and the required maximal L1 trigger system latency is 5μs, the TPG has available 3.5 μs of the total time budget to complete all its tasks. The basic TPG system should operate with a trigger-cell selection threshold of at least 2 MIP_T, an average pileup of 200 and the expected noise levels after an integrated luminosity of 3000 fb^{-1}.

The general two-stage architecture of the TPG system is given in Figure 2. In the first stage 2D clusters are formed, while the final 3D clusters are created in the second stage. Each endcap will have 14 sensitive layers in the CE-E section and 24 in the CE-H section. In the second stage the 24-fold time multiplexing is used in order to have all the 2D clusters and energy maps for a bunch crossing in one location.

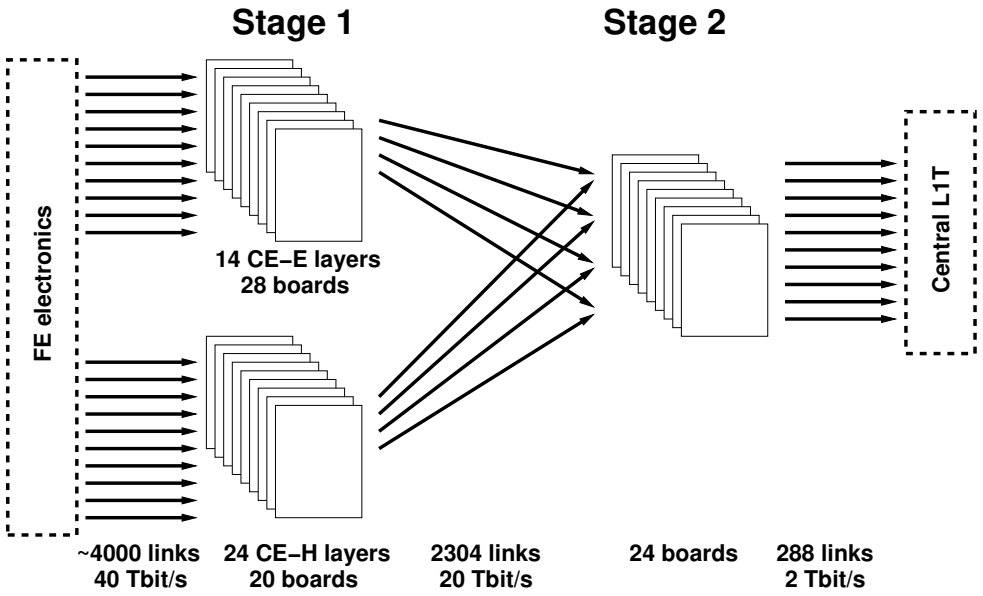

Figure 2. Two-stage architecture of the TPG system.

The TPG will be implemented using ATCA boards with one FPGA per board. In the first stage a total of 48 boards per endcap is used. The outputs from these boards will be transmitted to the boards in the second stage on 2304 links per endcap running at 16 Gbit/s. The second stage consists of 24 boards per endcap, each providing a processing node for a 24-fold time multiplexed system. These boards compute the 3D clusters, the energy map data per layer and a total transverse energy map. Each of the 24 boards in the second stage will then transmit the

output data over twelve 16 Gbit/s links to the central L1T system, requiring 288 links per endcap.

The two endcaps will function independently with identical copies of the hardware. A preliminary implementation of the VHDL for the 2D clustering algorighm indicates that it is feasible to have an overall TPG system latency within the required 3.5 μs.

4. Conclusion and outlook

The CMS collaboration is building a new generation of endcap calorimeters for the HL-LHC. The high granularity calorimeter will use a combination of silicon and scintillator-SiPM technologies to meet the requirements for high radiation tolerance, fast operation in high pileup environment and to enable efficient and precise particle identification in the forward region.

The basic electronics architecture has been defined, and work has started on the detailed design of the necessary ASICs and boards, as well as the algorithms to implement in the off-detector electronics.

Preliminary results from the test beam [9], ASICs tests and VHDL implementation show that the chosen architecture is promising in meeting stringent requirements for the HGCAL.

Acknowledgments

This work is supported by Croatian national foundation grant number 7118.

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