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Readout board upgrade for the Pixel Detectors: reasons, status and results in ATLAS

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The increase of luminosity in the LHC accelerator at CERN constitutes a challenge for the data readout since the rate of data to be transmitted depends on both pileup and trigger frequency. In the ATLAS experiment, the effect of the increased luminosity is most evident in the Pixel Detector, which is the detector closest to the beam pipe. In order to face the difficult experimental challenges, the readout system was upgraded during the last few years. The main purpose of the upgrade was to provide a higher bandwidth by exploiting more recent technologies. The new readout system is composed by two paired electronic boards named Back Of Crate (BOC) and ReadOut Driver (ROD). In this work the main readout limitation related to increased luminosity will be discussed as well as the strategy and the technological solutions adopted in order to cope with the future operational challenges. In addition the general progresses and achievements will be presented.

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1. A new readout system for IBL

Insertable B-Layer (IBL) [1] is the innermost and most recent layer of the ATLAS [2] Pixel Detector [3]. It was installed during the 2013-2015 long shutdown to increase the tracking robustness against failures as well as to improve the reconstruction precision even at the higher LHC luminosities. A new front-end chip, called FEI4 [4], was developed to be more radiation hard and to take the larger occupancy and bandwidth into account.

The off-detector electronics used in the original layers of the Pixel Detector, consisting of two VME boards called Silicon Read-Out Driver (SiROD) and Silicon Back Of Crate (SiBOC), featured obsolete components (Spartan 3 FPGAs), limited bandwidth (1.04 Gbps per pair), limited VME bus speed (used for calibration) and limited control and recovery mechanisms. For these reasons, the previous off-detector readout was unsuited to interface with the IBL and the development of a new, faster one was required. Two new 9U-VME cards were developed; IBLBOC and IBLROD [5] (also called simply BOC and ROD) implementing optical I/O interface and data processing respectively. The new readout system provides a bandwidth of 5.12 Gbps and communication through the software facilities is mediated by an embedded processor inside the ROD board, a PowerPC (PPC), which provides the system a high level monitoring and recovering tools.

2. Readout upgrade for all the Pixel Detector Layers

In a critical system such as the ATLAS Pixel Detector, situated very close to the beampipe, the bandwidth plays a key-role. The bandwidth must be higher than the throughput (the total amount of data to be sent per second), which is strictly influenced by the pile-up and the trigger rate. The ratio between bandwidth and throughput is called link occupancy; a link occupancy higher than 100% will lead to data loss and desynchronization. The old readout electronics (SiBOC and SiROD) limited bandwidth is shared between multiple modules: each VME pair can interface 26 Layer-2 modules at a readout speed of 40 Mbps, 13 Layer-1 or Disk modules at a readout speed of 80 Mbps or 6 B-Layer modules at a readout speed of 160 Mbps. The costant increase of luminosity and pileup leads to the increase of throughput and eventually to link saturation. One way to avoid this situation without changing detector configurations is to increase the system bandwidth and the readout speed of each module; the (IBL)BOC and (IBL)ROD, designed to interface the IBL, proved to be an optimal replacement to the previous readout, because the bandwidth provided was enough to double the module readout speed without doubling the number of readout boards. Table 1 shows the effects in terms of link occupancy of the readout upgrade. This upgrade started in 2015-2016, were all the Layer-2 readout (the most critical one) was replaced with the new one, doubling the module readout speed (from 40 Mbps to 80 Mbps). The same year 6 out of 38 Layer-1 boards were upgraded, without changing the readout speed. This way it was possible to perform a direct comparison between the old and the new readout under the same environmental conditions. The results of this comparison will be discussed in Section 4. In 2016-2017 all the Layer-1 readout was upgraded, doubling the module readout speed (from 80 Mbps to 160 Mbps). In 2017-2018 the Disks SiRODs will be replaced as well as the B-Layer ones. In the latter case the readout speed (already at the limit for the module) will not increase, but the number of RODs required will be halved and the system will be uniformed.

3. New readout overview

The ATLAS Insertable B-Layer (IBL) and Pixel Detector readout chain is composed by several components. The Timing and Trigger Control (TTC) Interface Module (TIM) interfaces the ATLAS Level-1 Trigger system signals to Pixel subdetectors. The front-end chips, Front-End readout chip FEI4 for IBL or FEI3 and Module Chip Controller (MCC) [6] for the other pixel layers, are bonded to the detector and send data via optical fiber to the readout electronics, 100 m from the detector. The readout electronics are composed of two boards: BOC, responsible for handling the control interface to and data from the detector while also providing the clock to the connected detector parts, and ROD, which processes data and sends commands to the front-end modules. The two boards are shown in Fig 1.

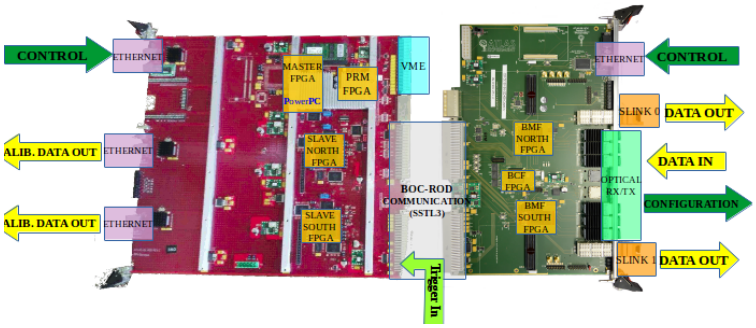


Figure 1: Part of the ATLAS Pixel Detector readout chain. The ROD board (on the left) features 3 Spartan-6 FPGAs (Program-Reset Manager (PRM), Slave North and Slave South) and one Virtex-5 FPGA (Master). The BOC board (on the right) features 3 Spartan-6 FPGAs (Board Controller FPGA (BCF), BOC Main Fpga (BMF) North and BMF South). The input-output connections are also shown in the figure.

4. Results

A link occupancy saturation (≈100%) leads to catastrophic consequences, since the readout chain is no longer capable to deal with all the incoming data. In this situation, the data received at the end of the readout chain will not be the expected one (i.e. the data will correspond to a different Level 1 trigger), and they will be flagged as desynchronized and ignored in the further steps of

Table 1: Module Link Occupancy estimation based on 2016 Run at different pileups (μ) assuming Level 1 trigger rate of 100 kHz and 13 TeV energy.

μ	Link Occupancy				
	B-Layer	Layer-1		Layer-2	
	both readouts (160 Mbps)	old readout (80 Mbps)	new readout (160 Mbps)	old readout (40 Mbps)	new readout (80 Mbps)
40	60%	81%	41%	**119%**	59%
60	81%	**103%**	52%	**159%**	79%
80	**101%**	**125%**	63%	**188%**	98%

event reconstruction. The efficiency in event reconstruction is thus strictly related to the amount of desynchronization, which itself depends on bandwidth, pileup and trigger rate.

The readout upgrade achieved its goal to provide enough bandwidth for the increasing luminosity of LHC while keeping the amount of desynchronized events under control, as it is show in Figure 2.

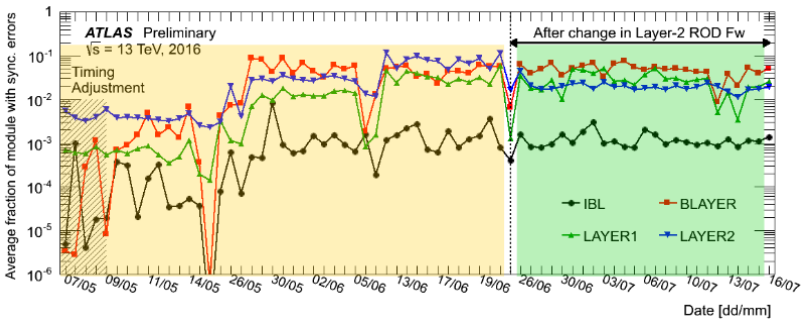
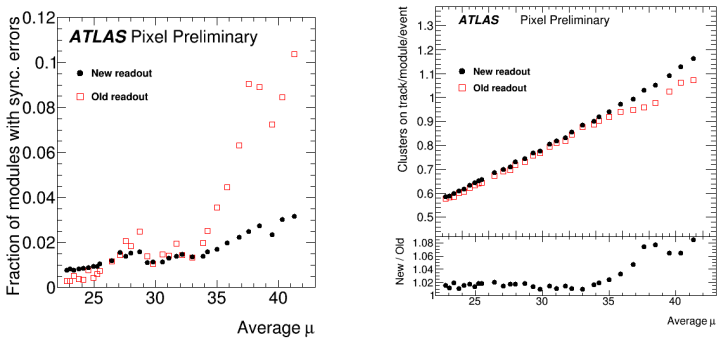


Figure 2: Fraction of modules with desynchronization errors for all the layers of the Pixel Detector after the readout upgrade of Layer-2 (2016). After a period of instability due to firmware bugs (orange section), it can be observed that the amount of desynchronization of Layer-2 (new readout) is comparable to or better than Layer-1 or B-Layer (old readout). For IBL the desynchronization is generally lower, thanks to a combined effect of the new front-end module and the new off-detector readout [7].

A direct comparison between the old and new readout was possible because in 2016 only 6 out of 38 boards were upgraded for Layer-1, without changing the module readout speed. The results are shown in figure 3.



(a) Fraction of modules with desynchronization error

(b) Clusters on track

Figure 3: The fraction of modules with synchronization errors and number of clusters on track per module per event as a function of pileup (μ) in the old and new readout at Layer-1 in fill 5446 in 2016. The new readout shows less synchronization errors with respect to the old readout in the same eta coverage, especially in the high pile-up region. This achievement was possible thanks to a mechanism that flushes FIFOs in the readout electronics at each Event Counter Reset (ECR), introduced for the new read-out in 2016. In 2017, this mechanism was also introduced for the old readout [8].

References

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