

The CMS ECAL data acquisition system and its performance at LHC Run 2

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> In 2017 the Large Hadron Collider at CERN has provided an astonishing 50 fb*−*¹ of proton-proton collisions at a center-of-mass energy of 13 TeV. The CMS detector has been able to record about 90% of this data. During this period, the CMS electromagnetic calorimeter (ECAL), based on 75848 scintillating PbWO4 crystals and a silicon and lead preshower, has continued exhibiting excellent performance with a very stable data acquisition system. The ECAL DAQ system follows a modular and scalar schema: the crystals are divided in sectors, each of them controlled by 3 interconnected boards. These boards are responsible for the configuration and control of the front-end electronics, the generation of trigger primitives for the central CMS first level trigger, and the collection of data. A multi-machine distributed software configures the electronic boards and follows the life cycle of the acquisition process. The ECAL electronics modular configuration is reflected in the software where a tree control structure is applied. Through a master web application, the user controls the communication with the sub-applications that are responsible for the off-detector board configurations. Since the beginning of Run 2 in 2015, many improvements to the ECAL DAQ have been implemented to reduce occasional errors, as well as to mitigate single event upsets in the front-end electronics, and to improve the efficiency. Efforts at the software level have been made to introduce automatic recovery in case of errors. These procedures are mandatory to have a reliable and efficient acquisition system.

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1. Introduction

The Large Hadron Collider (LHC) delivered about 50 fb*−*¹ of proton-proton collisions at a centre-of-mass energy of 13 TeV during 2017 at interaction point 5. The Compact Muon Solenoid (CMS) detector has been able to record 90.3% of this data [1].

CMS features a hermetic electromagnetic calorimeter [2] (ECAL), composed of 61200 lead tungsten crystals in the barrel and 7324 in each endcap, and a preshower endcap detector (ES) aimed at π^0/γ separation and composed of two layers of thin lead converters, each followed by a silicon strip detector plane.

2. ECAL DAQ

2.1 Front End electronics

The basic detector unit of the ECAL is the *trigger tower* (TT) [3], which is a group of 25 adjacent crystals. Every trigger tower is controlled by a group of on-detector boards, called *Front End*, that process at 40 MHz the data received from the sensors attached to the crystals. It is composed of a motherboard, five *Very Front End* (VFE) cards and a *Front End* (FE) card.

The front end electronics is the first step of both the Trigger and the Data Acquisition (DAQ) paths. It shapes, amplifies and digitalises the signals from the photodetectors, generates the trigger primitives that are used in L1 Trigger decision, stores the crystals full granularity data in buffers waiting for the L1 Trigger decision and ready to be sent to the next DAQ step.

EFcard FENIX chip in
"STRIP mode' VFF card Lead-Tungstate crystals FENIX chip "TCP" mode FENIX chip in
"DAQ" mode 。
Gigabit Links (GOH) Trigger Data Readout Data Clock and Control .
AD41240 ADC Multi-Gain Pre-Amplifier chip (MPGA) Clock and Control Chip (CCU)

(a) ECAL and ES subsystems: EB (ECAL barrel) in green, EE (ECAL endcap) in blue and ES (ECAL preshower in red)

(b) Schema of the Front End electronics

2.2 Off-detector electronics

The front end electronics is divided in sectors (FED), each of them managed by three interconnected boards.

The *Trigger Concentrator Card* completes the trigger primitive generation and sends the trigger data to the Regional Calorimeter Trigger through the *Synchronization and Link Board* (SLB), which synchronizes the trigger primitives since the different particle flight in the detector introduces non-negligible differences in their timings. Moreover, the TCC board classifies the trigger towers in high, medium and low interest and sends this data to the *Selective Readout Processor* (SRP).

The *Clock and Control System* (CCS) board is responsible for the configuration and the control of the front-end electronics. The synchronization of the on-detector and off-detector boards with the LHC bunches is essential to assign the data to the right bunch-crossing. The CCS distributes the commands coming from the *Trigger Control and Distribution System* (TCDS) to the other offdetector boards through the backplane of the crate and to the front end electronics using dedicated optical links called *token rings*. These commands include the L1 Accept and triggers for calibration and tests, the *Trigger and Timing Control* (TTC) system, which distributes the CMS central clock, and the *Trigger Throttling System* (TTS), which limits the rate in case of buffers of the electronics that may overflow.

After receiving a L1 Accept command, the *Data Concentrator Card* (DCC) collects the fullgranularity crystal data from the FE boards through dedicated optical links and the trigger primitives from the TCC through the backplane of the crate. Then the DCC performs integrity checks of the data collected and receives information from the SRP, which allows the DCC to save bandwidth by applying a suppression algorithm to the data from the trigger towers that are considered not to contain interesting events. Eventually, the DCC sends the data to the central DAQ.

Figure 2: ECAL on-detector and off-detector electronics schema. Trigger path in green, control path in blue, and DAQ path in red

2.3 Online software

The ECAL online software is responsible for the configuration, operation and monitoring of the ECAL trigger and data acquisition system. The software has been developed as a modular distributed system based on XDAQ libraries [4], which provide the basic services necessary by the online DAQ system using web technologies and network communication protocols. It configures the hardware according to the parameters saved on the configuration database, configures the ECAL calibration monitoring system and monitors the hardware during data acquisition.

The ECAL software has a hierarchical and modular structure and it is built around a *Finite State Machine* that defines the life-cycle of every software component. At the top level there are the *Function Managers* (FM), web applications based on the *Run Control and Monitoring System* Java framework. The FMs are the most external layer of the system and are exposed to the action of the operator. They are responsible for managing the life-cycle of the lower layer applications. The Level-0 Function Manager controls a Function Manager for each subsystem. From the FMs it is possible to chose the software and hardware configurations. Moreover, all the errors are reported to the top FM for a quick operator's response.

The building blocks of the ECAL software are the *ECAL Supervisor* and the *Resource Supervisors*. The ECAL Supervisor receives the commands from the ECAL FM and dispatches them to the Resource Supervisors. For every type of off-detector board a specific Resource Supervisor has been implemented. Every board is controlled by a single instance of the corresponding Resource Supervisor, which retrieves the configuration parameters from the database according to the directives of the ECAL Supervisor, then configures and monitors the board.

Figure 3: ECAL Online Software schema

2.4 Monitoring software

Additional web monitoring software has been implemented in order to have an online overview of the status of the electronics and to keep track of the errors, to help the offline analysis of the problems that may occur during datataking. These applications are based on the informations coming from the Resource Supervisors and collected by the Slash XDAQ server. They consist in a *nodejs* backend that exposes a REST API and frontend *VUEjs* components.

3. Improvements and performance of ECAL DAQ

In order to reduce the downtime caused by ECAL DAQ, several action have been undertaken in both ECAL and ES.

In 2016, ECAL already had a *Single Event Upset* recovery system acting on the on-detector electronics. It relies on the DCC board recognizing the FE error and communicating it to its supervisor, which asks the ECAL Supervisor to pause the run, then manages the on-the-fly recovery of the electronics and eventually asks for the run to restart.

From 2017, the same procedure has been used to recover from a wider range of FE electronics errors and from known errors of the off-detector electronics, which helped reducing the downtime caused by ECAL DAQ.

Figure 4: Diagram of the SEU recovery procedure

In 2017, the SEU recovery procedure acting on the on-detector electronics has been implemented also in ES, greatly improving ES DAQ performance. Moreover, the automatic masking of the faulty ES DCC channels has been deployed. A similar system has been deployed in ECAL in 2018.

The positive effect of the aforementioned actions manifest in the reduction of luminosity loss induced by ECAL ans ES DAQ systems of about 36% and 76% respectively, as appears in Table 1.

	Year LHC delivered (fb^{-1}) CMS recorded (fb^{-1})		ECAL DAQ - induced losses
			$ECAL + ES$ (pb ⁻¹ (% of LHC delivered))
2016	41.07	37.82	$237.12 + 189.23 (0.6\% + 0.5\%)$
2017	50.25	45.39	$151.57 + 45.12(0.3% + 0.09%)$

Table 1: All the data has been gathered from [1].

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