PROCEEDINGS OF SCIENCE

A PCI Express board proposed for the upgrade of the ATLAS TDAQ read-out system

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During the next years a great number of laboratories all around the world will be involved in the upgrading of the main experiments at CERN's LHC (ATLAS, CMS, LHCb, ALICE). The ATLAS Bologna group, which collaborates with the Pixel Detector DAQ, in the last two years has developed a prototype of a new board named PILUP (PIxel detector high Luminosity UPgrade); this board is a candidate for the redesign of the ATLAS DAQ required for High Luminosity LHC project. The main characteristics of this board are the embedded processor (dual-core ARM) and the large communication bandwidth (up to 60 Gb/s through optical fibers). The board is hence capable of managing complex systems and data transmissions suitable to meet the performance required to reach the next High Energy Physics goals. The PILUP has already demonstrated the capability to manage the communication with the main board of the ATLAS DAQ upgrade, the FELIX, using different communication protocols (GBT and Full-Mode). This is the first result of the collaboration with the FELIX group. Moreover, its features make it adaptable to be programmed as an emulator of several devices (front end electronic or read-out chips like the new RD53a). In conclusion, the characteristics of this new board and the experience of its team of developers open many directions for the use of the PILUP.

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1. Introduction

The Large Hadron Collider (LHC) accelerator operating at CERN will undergo a Long Shutdown (its second) in the next years. After this phase the system will reach an instantaneous luminosity of $5 \times 10^{34} \mathrm{cm}^{-2}\mathrm{s}^{-1}$ and an integrated luminosity of 300 fb^{-1} [1], thus increasing the amount of data to be managed by the read-out system (e.g ATLAS, from 100 kHz to $\sim$1 MHz). The experiments at the LHC, of course, will undergo an upgrade phase as well, and the argument of this PoS is a proposal for the upgrade of the ATLAS Pixel Detector TDAQ read-out system. In particular it will be introduced and discussed a new PCI Express based electronic board developed in collaboration by the University of Bologna and the INFN (Istituto Nazionale di Fisica Nucleare). This board, named PILUP (Pixel detector hl-Lhc Upgrade), is based on a SoC (System on a Chip) and a FPGAs produced by XILINX: a Zynq-7000 [2] and a Kintex-7 [3], in Master-Slave configuration. After July 2017 the group of people involved in the design of the PILUP board started a collaboration with those developing the main board meant to the ATLAS upgrade, named FELIX [4]; this led to the Protocol Converter, system that will be discussed later. Seven PILUPs boards have been produced and completely tested so far, two in its version 1.0 and five in version 1.1 (shown in Figure 1).

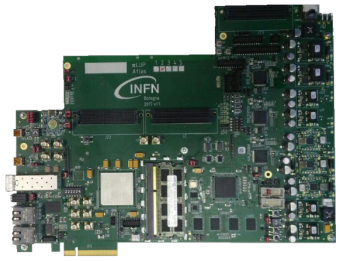

Figure 1: PILUP version 1.1.

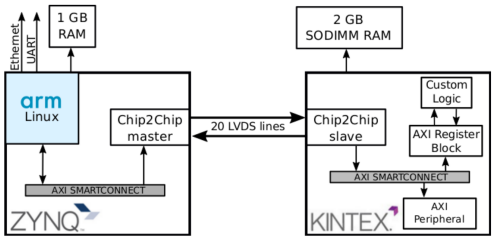

Figure 2: PILUP firmware architecture.

2. PILUP

The PILUP project started in 2015 and is being carried out by the Bologna group which made the upgrade of the current read-out system of the ATLAS Pixel Detector front-end [5], with the purpose to upgrade it. The PILUP is based on a Master-Slave architecture controlled by an embedded dual-core ARM Cortex A9 CPU with a clock frequency of 800 MHz. Mounted on the Zynq and the Kintex managed parts of the board there are (one at each side): a UART port, a 1 Gb/s Ethernet port, a FMC (FPGA Mezzanine Card) LPC (Low Pin Connector), a fixed clock source at 200 MHz, a Si570 clock generator (10 to 810 MHz), a 32 MB flash memory and a 1 GB of RAM memory. The Kintex-7 takes care of the data management, and mounts: a 128 MB flash memory, an Ethernet port up to at 10 Gb/s ("transceiver", see later), a fixed clock source at 125 MHz, a Si5326 jitter cleaner and clock generator, and a FMC HPC (High Pin Connector). There are 16 GTX [6] high performance serializers (called "transceivers"), which allow a total bandwidth of 200 Gb/s (12,5 Gb/s each one), where half of them are dedicated for the PCI Express [7] bus 8x Generation 2 (4 GB/s of bus bandwidth saturated up to 3,2 GB/s), while the others are divided into a coaxial connection, a optical fibre, and 2 FMC connectors - a HPC and a LPC (in total 5 of the

Transceivers	Throughput	Bit Error Rate	Eye Diagram Open Area
FMC HPC (SFP+)	10 Gb/s	$\leq 10^{-14}$	$\simeq 10^4$(5 Gb/s), $\simeq 2\times 10^3$(10 Gb/s)
SFP+	10 Gb/s	$\leq 10^{-14}$	$\simeq 10^4$(5 Gb/s), $\simeq 2\times 10^3$(10 Gb/s)
SMA	12,5 Gb/s	$\leq 10^{-14}$	$\simeq 2\times 10^3$(5 Gb/s), $\simeq 5\times 10^2$(10 Gb/s)

Table 1: PILUP tests highlights.

16 transceivers are assigned in these connectors)- which allow to use multiple types of fast connections. The Zynq-7000 and the Kintex-7 communicate through a 21 bits differential synchronous bus running at the maximum tested speed of 200 MHz DDR (Double Data Rate). The testing phase of 5 new PILUPs version 1.1 was concluded in the early 2018; in Table 1 the highlights of the tests are shown. The firmware structure of the board is shown in Figure 2. The AMBA AXI protocol used for the communication is extended between the FPGAs through the AXI Chip2Chip IP core provided by XILINX. This core bridges a 32-bits AXI bus to the slave device so that any peripheral present in the Kintex can be addressed from the ARM as if it was directly implemented in the Zynq. The communication is possible thanks to 20 differential lines operating at 200 MHz DDR. The Chip2Chip performs an automatic de-skewing calibration. The ARM runs an embedded Linux distribution generated with the XILINX Petalinux tools, providing a high level interface to any functionality present in the board (including some web services such as an SSH server). This high-level system (firmware and software) can be loaded from the Zynq flash memory or downloaded from a remote server with the Trivial File Transfer Protocol (TFTP) protocol. Most of the AXI cores offered by XILINX can be used thanks to drivers released by the core producer and already implemented in the Linux kernel tree; for custom-made cores without an AXI interface a control interface is offered by an AXI-addressable register block that is directly accessed from Linux user-space using the generic-UIO driver.

3. Proposed Application

The PILUP has been proposed as part of the ATLAS TDAQ read-out system for the new RD53a front-end chip [8] that will upgrade the Pixel detectors of ATLAS and CMS. Four types of data protocol have to be handled in order to set up the communication between the FELIX cards and RD53a: the GBT protocol [9] developed by CERN (output of the FELIX, with bandwidth of 4,8 Gb/s) and the Full-Mode protocol developed by the FELIX group (input of the FELIX, with bandwidth of 9,6 Gb/s), which are the protocols used by the FELIX cards, the Aurora 64b/66b protocol (output of the RD53a, with a bandwidth of 5,12 Gb/s divided in 1,28 Gb/s for each of 4 lanes) and a 160 Mb/s data lane (input of the RD53a) for the RD53a. To test the chip will be used a Single Chip Card (SCC) with the RD53a mounted on it. The FELIX card transmits over optical fiber technology, using SCC through Display Port (DP) connectors. The role of the PILUP is to act as a bridge between these 2 systems, handling both the "FELIX to RD53a" data-path (downlink) and the "RD53a to FELIX" path (uplink). The firmware architecture that accomplishes this task is shown in Figure 3. The PiLUP card allows two distinct protocol conversions: the output of the FELIX cards (GBT) to a 160 Mb/s data stream; the Aurora 64b/66b to the Full-Mode protocol. The hardware set up is shown in Figure 4. Two FMC mezzanines are used: the FM-S14 [10] for

the optical communication between FELIX cards and PILUP and the Single Chip Adapter [11] for the communication between PILUP and SCC through DP.

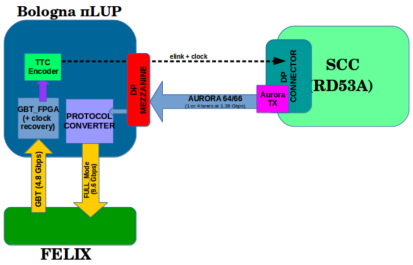

Figure 3: Scheme of the Protocol Converter firmware.

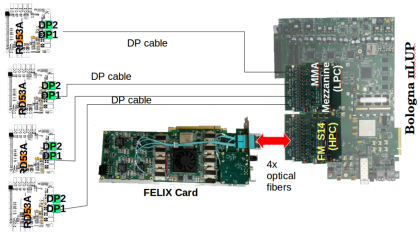

Figure 4: Proposed hardware setup.

4. Conclusions

The Bologna group has developed a new PCI Express based board named PILUP, which has the potential to become an important component of the future TDAQ upgrade of the ATLAS experiment. Multiple collaborations with national and international institutions such as the FELIX group and the University of Lecce have started and two PILUPs have been shared among different places (the Brookhaven National Laboratory and the Lecce University).

References

[1] B. Schmid, *The High-Luminosity upgrade of the LHC: Physics and Technology Challenges for the Accelerator and the Experiments*, J. Phys.: Conf. Ser 706, 022002, 2016.

[2] XILINX, *Zynq-7000 SoC, Technical Reference Manual*, UG585(v1.12.2), July 1, 2018.

[3] XILINX, *KC705 Evaluation Board for the Kintex-7 FPGA User Guide*, UG810 (v1.8.1), July 10, 2018.

[4] J. Anderson, K. Bauer et al., *FELIX: a PCIe based high-throughput approach for interfacing front-end and trigger electronics in the ATLAS Upgrade framework*, Journal of Instrumentation, vol. 11, pp C12023, 2016..

[5] N. Giangiacomi [ATLAS Collaboration], *Readout board upgrade for the Pixel Detectors: reasons, status and results in ATLAS*, PoS EPS-HEP2017 790, 2018.

[6] XILINX, *7 Series FPGAs GTX/GTH Transceivers User Guide*, UG476 (v1.12.1), August 14, 2018.

[7] R. Budruk, D. Anderson, T. Shanley, *PCI Express System Architecture*, Pearson Education (US), 2003.

[8] N. Demaria et al., *Recent progress of RD53 Collaboration towards next generation Pixel Read-Out Chip for HL-LHC*, Journal of Instrumentation, vol. 11, pp. C12058, 2016.

[9] S. Muschter, S. Baron, C. Bohm, J. P. Cachemiche and C. Soos, *Optimizing latency in Xilinx FPGA implementations of the GBT*, Journal of Instrumentation, vol. 5, pp. C12017, 2010.

[10] Faster Technology, *FM-S14 User Manual*, November 5 2014.

[11] https://twiki.cern.ch/twiki/pub/RD53/RD53ATesting/FMC_adapter_card_for_single_chip_testing_V1.0.pdf