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ATLAS Calorimeter system: Run-2 performance, Phase-1 and Phase-2 upgrades

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The ATLAS detector was designed and built to study proton-proton collisions produced at the LHC at centre-of-mass energies up to 14 TeV and instantaneous luminosities up to $10^{34}\text{cm}^{-2}\text{s}^{-1}$. A liquid argon sampling calorimeter (LAr) is employed as electromagnetic calorimeter and hadronic calorimeter, except in the barrel region, where a scintillator-steel sampling calorimeter (TileCal) is used for the hadronic calorimeter.
ATLAS recorded 87fb^{-1} of data at a center-of-mass energy of 13 TeV between 2015 and 2017. The calorimetry system performed accordingly to its design values and played a crucial role in the ATLAS physics programme.
This contribution gives an overview of the detector operation, monitoring and data quality, as well as the achieved performance, including the calibration and stability of the energy scale, noise level, response uniformity and time resolution of the ATLAS calorimetry system. The upgrade projects of the ATLAS calorimeter system are presented.
An upgrade of the LAr trigger readout is necessary for Run-3, where luminosities around $\mathscr{L} \approx 2-3 \times 10^{34}\ \text{cm}^{-2}\text{s}^{-1}$ will be achieved, in order to keep a high signal efficiency. The electronics includes the LAr Trigger Digitizer front-end system that digitizes 34,000 channels at 40 MHz with transverse 12-bit precision after bipolar shaping and the back-end LAr Digital Processing system that computes the energy and time of the signals. Results of the system integration tests are presented along with the overall system design.
For the high luminosity phase of the LHC (HL-LHC), the luminosity will increase up to $\mathscr{L} \approx 7.5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ leading to an average pile-up up to 200 interactions per bunch crossing. The electronics of both calorimeters has to be upgraded to cope with longer latencies of up to 35 μs needed by the trigger system for such high pile-up levels.
For the Tile system, the photomultiplier signals will be digitized and transferred off-detector to the TileCal PreProcessors (TilePPr) for every bunch crossing, requiring a data bandwidth of 40 Tbps to read out the entire detector. The TilePPr will reconstruct, store and send the calorimeter signals to first level of trigger at a rate of 40 MHz. In parallel, the data samples will be stored in pipeline memories until the reception of the first-level trigger acceptance signal. The data of the selected events by the ATLAS central trigger system will be transferred to the ATLAS global Data AcQuisition (DAQ) system for further processing.
Test results of the first prototypes will be presented, along with design studies and simulations of the performance of the readout system.

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1. The ATLAS calorimeter performance

The main purpose of the calorimeters is the reconstruction of electrons, photons, jets and MET and hence data quality, energy scale and resolution are crucial for many physics analyses. Offline LAr Data Quality efficiency in 2017 has been excellent again; only 0.03 % of data were rejected by event vetoing and only 0.62 % (299 pb^{-1}) were lost due to lumi-block rejection. In 2015, 2016 and 2017, the overall efficiencies of ATLAS were 87.1 %, 93.0 % and 93.6 %; while for LAr they were 99.4 %, 99.8 % and 99.5 % and for Tile, 100.0 %, 98.8 %, and 99.4 %. Figure 1 shows the luminosity losses by LAr per period and the reason. One reason for rejecting data is coherent noise.

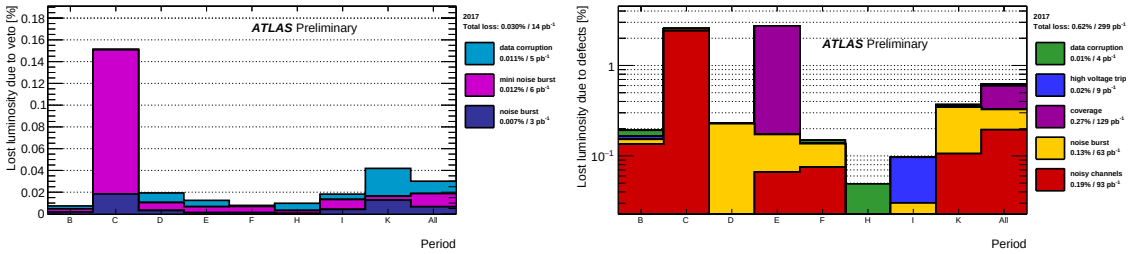

Figure 1: LAr data quality: Luminosity loss due to event veto (left) and the reason for rejecting data (right).

It is distinguished from Noise Bursts (a brief increase in noise over a large region that affects the end-caps and has a duration of: 1 μs - 1 ms) and Mini Noise Bursts (a burst seen in $\mathcal{O}(10)$ nearby channels, mainly in the barrel and with a very short duration: < 1 μs). They are identified by a bad quality factor and are treated by vetoing time periods (1 ms) around the noise burst candidate. If too many noisy events are detected, then the entire lumi block is rejected. Figure 2 left shows an example. Tile calorimeter noise is regularly measured with a complex calibration system. Run-2 improvements resulted in the stability of the absolute energy scale at cell level being maintained to be better than 1%. New Low Voltage Power Supplies show less electronic noise, there is increased stability and safety for the Cesium calibration procedure, upgraded laser electronics better control the emitted light and redundancy of the cell readout system reduces the impact of masked channels (see Figure 2 right).

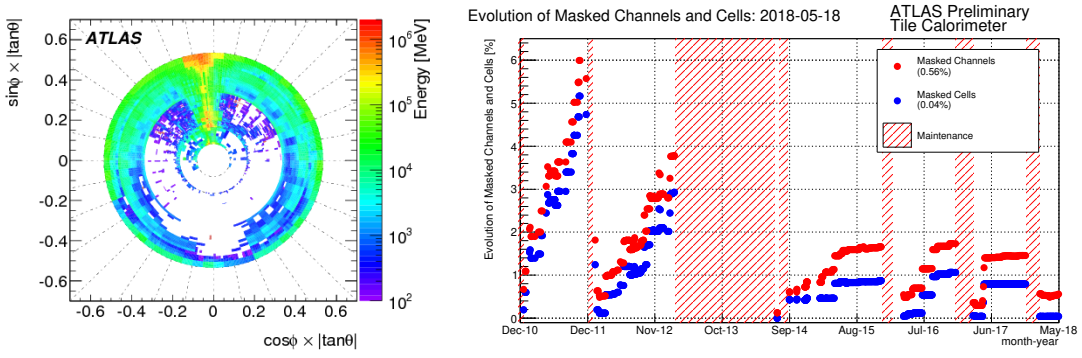

Figure 2: Left: Example of LAr noise burst (end cap), Right: Tile masked channels in Run-2.

2. Phase-1 upgrade: Upgrade of LAr trigger readout

The LAr Phase-1 Upgrade [1] for Run-3 has 124 LAr Trigger Digitizer Boards (LTDB) on the

front-end that read out new SuperCell trigger primitives as shown in Figure 3 left. Their off-detector counterpart will be 31 LAr Digital Processing Blades (ATCA technology) for energy reconstruction and data buffering, each with 4 FPGA-equipped Advanced Mezzanine Cards (AMC). In 2014, a first Demonstrator was installed (Figure 3 right). Recently, the final board production has started.

The full installation will be done in LS2 followed by commissioning. The installation of new FE baseplanes will be especially challenging since all 1524 Front-end Boards have to be removed and re-installed. This system will remain operational during the HL-LHC period.

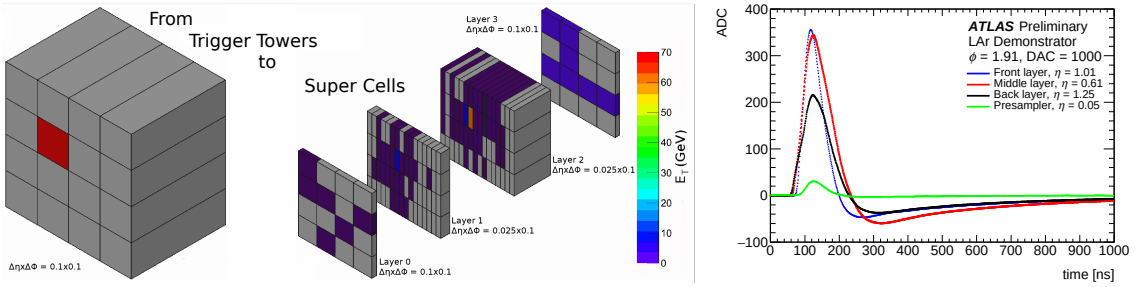

Figure 3: Left: new Super-Cell (SC) primitives; Right: SC pulse shapes of LAr Demonstrator.

3. Phase-2 upgrade: New Tile readout

The Phase-2 upgrade uses a new trigger paradigm based on a 40 MHz full granularity readout with an increased L0 trigger rate of 1 to 4 MHz and pipeline memories of up to 35 μs. For TileCal [2] this implies a replacement of the full readout electronics, both on- and off-detector, as sketched in Figure 4, with 4096 up-links (9.6 Gbps) and 2048 down-links (4.8 Gbps). A new

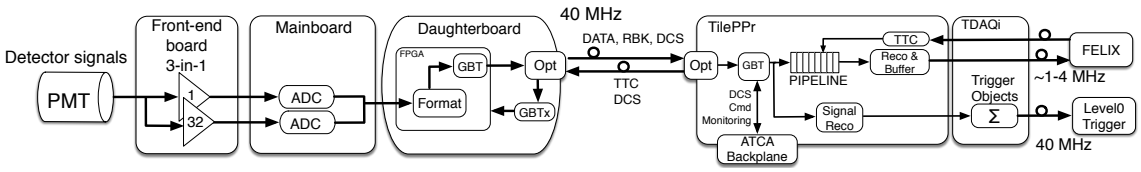

Figure 4: Tile readout block diagram for the Phase-2 Upgrade.

concept of MiniDrawers (Figure 5 left), where 4 MiniDrawers compose a SuperDrawer, will allow better accessibility of electronics for maintenance. A fully functional Demonstrator has been tested intensively during 6 test beam campaigns. A total of 32 ATCA carrier blades, each with 4 Compact Processing Modules (CPM) AMC boards, will serve as back-end. Each CPM will connect to 8 MiniDrawers and carry out the digital filtering and data buffering until there is an L0/L1 accept. For this the Xilinx Kintex Ultrascale is under study as a candidate FPGA. The Trigger DAQ interface module (TDAQi) will prepare digital trigger sums and connect to the trigger Feature EXtractor (FEX) modules. Full granularity data above a noise threshold ($> 2\sigma$) will be available for the Global Event trigger. Preliminary results from radiation hardness testing for all major components are available but more tests are needed to satisfy the exact ATLAS rules for irradiation. The first full size Tile PreProcessor (carrier + CPMs) is expected by end of 2018 and a possible insertion of the Demonstrator module in ATLAS during LS2 is currently being discussed.

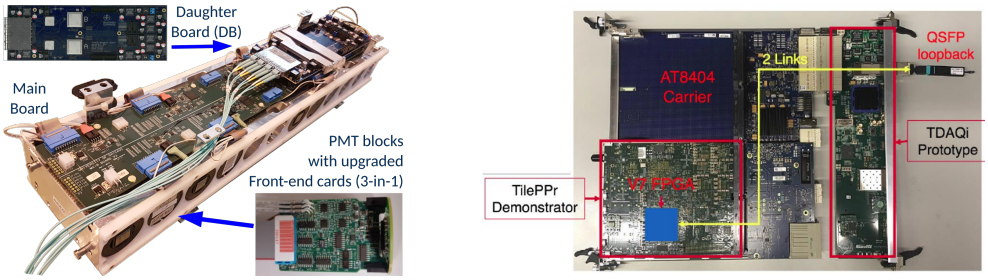

Figure 5: Tile Phase-2 electronics: MiniDrawer (front-end, left) and TilePPr with TDAQi (back-end, right).

4. Phase-2 upgrade: New LAr readout

Similar to the Tile calorimeter, a full replacement of the detector readout electronics is planned for LAr [3]. It will comprise 1524 new Front-end Boards (FEB2: 128 channels each), 130 Calibration Boards, new FE power; and will keep the Phase-I SuperCell readout for the L0 trigger.

Digitisation on the FEB2s by a 2-gain readout and 14-bit ADC for 16-17 bit dynamic range is targeted in order to keep electroweak physics signals in same gain range. A second iteration pre-prototype implementation, called a COLUTA ASIC (Figure 6 left), has been submitted in June 2018. The specification of 11.2 ENOB (Effective Number Of Bits) is close to being met. It uses a Dynamic Range Enhancer (DRE) with internal 4x gain and a 12-bit pipeline Successive Approximation Register (SAR) ADC to reach the 14 bit specification. The back-end foresees 372 new LAr Signal Processors (LASP) that will replace the current Read Out Drivers. For a LASP board, a full-size ATCA blade with 2 processing FPGAs is proposed, each handling the incoming data from 4 FEB2s. It will receive digitised FEB2 data, apply digital filtering, buffer the data and await the trigger decision before finally transmitting the triggered data to the DAQ system (Figure 6 right). The main challenges are ATCA power consumption and cooling for which studies are ongoing.

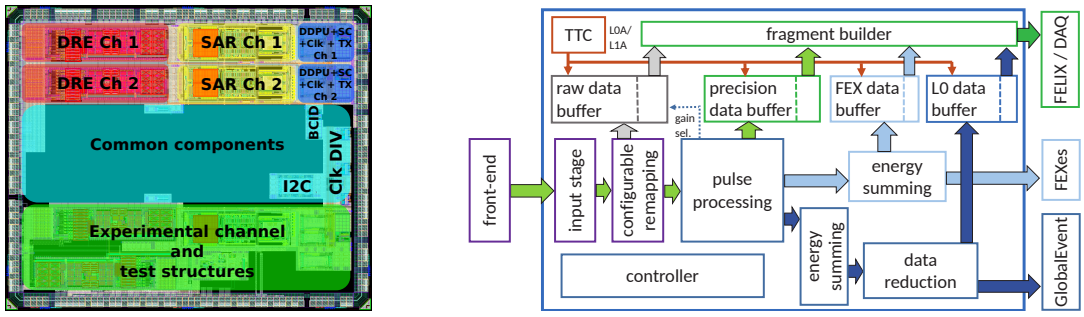

Figure 6: LAr Phase-2 electronics: COLUTA chip (left) and LASP function blocks (right).

References

[1] M. Aleksa, W. Cleland, Y. Enari, M. Fincke-Keeler, L. Hervas, F. Lanni et al., *ATLAS Liquid Argon Calorimeter Phase-I Upgrade Technical Design Report*, Tech. Rep. CERN-LHCC-2013-017. ATLAS-TDR-022, CERN, Geneva, Sep, 2013.

[2] ATLAS Collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter*, Tech. Rep. CERN-LHCC-2017-019. ATLAS-TDR-028, CERN, Geneva, Sep, 2017.

[3] ATLAS Collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS LAr Calorimeter*, Tech. Rep. CERN-LHCC-2017-018. ATLAS-TDR-027, CERN, Geneva, Sep, 2017.