

Front-End and Back-End Electronics for the ATLAS New Small Wheel Upgrade

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The upgrades of the Large Hadron Collider (LHC) at CERN and the experiments in 2019-20 (LS2) and 2024-26 (LS3) will allow to increase the instantaneous luminosity. During LS2, each of the so-called "Small Wheels" of the ATLAS muon spectrometer are planned to be replaced by the "New Small Wheel" (NSW), which will be comprised of two gaseous detector technologies, namely the Micromegas (MM), mainly used for track reconstruction and the small strip Thin Gap Chambers (sTGC), mainly used for triggering. The 2.4 million readout channels of those chambers will require a new generation of electronics to read them out, that will be able to endure a harsh radiation environment while at the same time be compatible with the Phase-II trigger rates, which are expected to reach a Level-0 frequency of 1MHz and a Level-1 frequency of 400kHz. Several custom Application-Specific-Integrated-Circuits (ASICs) have been developed for the electronics system of the NSW, besides special boards to house these ASICs, as well as dedicated Field-Programmable Gate Array (FPGA) designs. A general overview of the main elements of the NSW electronics scheme is provided here.

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1. Introduction

The NSW will provide data for offline track reconstruction, mainly through the MM detector, that can deliver a spatial resolution as low as $100\ \mu\text{m}$ [1] and trigger candidates to ATLAS, mainly through the sTGC, with a precision of approximately 1-2 mrad. In addition, the MM chambers may provide trigger primitives as well, while the sTGC can also contribute to precision tracking. This fully redundant system, is being readout by the VMM, a mixed-signal ASIC [2], that directly connects to the vast number of readout elements of both detector technologies. The overall NSW trigger and readout scheme can be examined in Fig. 1, where one can see the rest of the components of the electronics system, such as readout or configuration-dedicated ASICs, other ASICs that handle trigger data and the boards that these chips are mounted on.

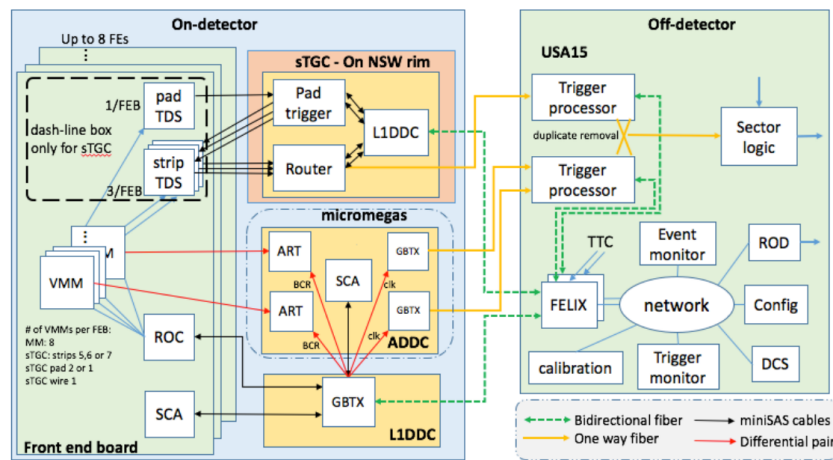


Figure 1: Overview of the NSW Electronics scheme. The front-end detector boards are depicted on the left (for MM and sTGC), the data-driver cards (L1DDC, ADDC) in the middle alongside the Pad Trigger and Router, while the back-end electronics can be seen on the right [1].

2. Readout Path - Precision Tracking

The VMM is a custom ASIC that can be used in a variety of charge interpolated tracking detectors, packaged in a Ball Grid Array with outline dimensions of $21 \times 21\ \text{mm}^2$. The chip is comprised of 64 discrete channels. Each channel connects to a detector readout element and performs charge amplification, discrimination and precise amplitude and timing measurements through Analog-to-Digital Converters (ADCs). The front-end amplifier can operate within a wide range of input capacitances, has adjustable polarity, gain and integration time. The chip also uses Triple Modular Redundancy (TMR) to protect itself from Single Event Upsets (SEUs) that are highly possible in the harsh radiation environment of the ATLAS small wheel region.

The VMM can provide a precise amplitude measurement of the input pulse encoded in a 10-bit word (PDO) and a precise timing estimation of the pulse's peak encoded in an 8-bit word (TDO). These muon-related-pulse data are calculated by the chip within 200 ns and stored in its L0 buffers, to-be-selected by another electronic device at a later stage, namely, the Read-Out Controller (ROC)

ASIC. The ROC is responsible for receiving the Level-0 Accept (L0A) signal from the back-end electronics of the ATLAS trigger and then forward this signal to the VMM. Precise timing of the L0A allows for cherry-picking interesting events related to muons, stored in the VMM's L0 buffers and discarding irrelevant data that have been induced by noise. The ROC then builds a packet from the event data received by the VMMs it is connected to and forwards the event towards the back-end via a serial electrical link, called E-link, at 320Mbps, upon the reception of the Level-1 Accept (L1A) signal.

For the MM chamber technology, the VMMs and the ROC are housed by the Micromegas Front-End Board (MMFE8), and for the sTGC, by the pad and strip Front-End Boards (pFEB and sFEB). The MMFE8 is connected to the MM readout strips, that have a pitch of about $400\mu\text{m}$, whereas the pFEB is connected to the sTGC's large pads (about $8 \times 8\text{cm}^2$ in size) and the sFEB to the dense sTGC strips (3.2mm pitch). All of the front-ends interface via the E-links with the Level-1 Data-Driver Card (L1DDC), a data aggregator board, that connects with up to eight front-ends. On the back-end, the L1DDC interfaces with the Front-End Link eXchange (FELIX) via optical fiber at a speed of 4.8Gbps. The main feature of the L1DDC is the GBTx [3] ASIC. The GBTx is a high-speed radiation-tolerant transceiver, that connects to several front-end ASICs (ROC for the NSW) via serial E-link connections, collects all data from these chips and forwards them towards the back-end via optical fiber. The connection is also bidirectional, that is, configuration data can be received from FELIX and driven to the front-end as well. These data are used by the Slow Control Adapter (SCA) ASIC, residing on each front-end board, to alter the functionalities of the VMM and ROC.

On the back-end of the readout path, lies FELIX. FELIX is an FPGA-based data-routing device, mounted on a board connected to a PCIe slot of a commercial PC [4]. The FPGA board interfaces via optical fiber with the GBTx chips of the front-end, collects the events from the optical links and eventually dumps the received data to the ReadOut Drivers (ROD). It also receives slow control data from the Detector Control System (DCS) and configures the front-end chips via the SCA. Finally, it distributes Trigger Timing and Control (TTC) signals to all front-end boards. These signals include the trigger bits L0A/L1A, as well as a common reference clock.

3. Trigger Path

The VMM can also operate at a faster mode, used for triggering. Upon the detection of a peak that crosses the user-defined threshold, the chip outputs the channel address that this peak was detected on. This is called the Address-in-Real-Time (ART) mode and is used in the MM trigger scheme. The VMM also has a fast digitization 6-bit ADC (6bADC), that provides a coarse, but rapid, amplitude measurement of the pulse encoded in 6-bits. In addition, as long as a pulse is above the threshold, the VMM outputs a single-bit Time-over-Threshold (ToT) flag in one of its 64 direct-timing output pins. The 6bADC data and ToT signals are used by the sTGC trigger electronics to determine trigger candidates. The VMMs on the pFEB operate in the ToT mode and the sFEB VMMs operate in the 6bADC mode.

One of the main elements of the sTGC trigger electronics is the Trigger Data Serializer (TDS) ASIC [5]. There are two types of TDS ASICs, one for the pFEB and one for the sFEB. The pFEB

TDS collects the ToT signals from all VMMs and timestamps them with the BCID. The sFEB TDS deserializes the 6bADC data from the VMMs on the board and buffers them temporarily. Connected to both FEBs is the Pad Trigger (PT) board, an FPGA-based processor that uses the ToT signals, that give a rough estimate of a muon event position, to create a Region-of-Interest (RoI). A continuous stream of ToT flags with their timestamps are sent by multiple pFEB TDSs to the PT and if a 3-out-of-4 coincidence is found by the PT in both sTGC quadruplets of a wedge, a RoI is formed. The PT then signals the sFEB TDS chips within that RoI to send out their buffered 6bADC data towards the sTGC Trigger Processor via the Router Board. This scheme, though complex, reduces throughput towards the sTGC Trigger Processor without compromising for precision.

On the MM trigger path side, only the ART mode is being used, resulting in a simpler scheme. The ART signals from the VMM are driven to the ART Data-Driver Card (ADDC) that connects with up to eight MMFE8s (thus, 64 VMMs). The ART ASIC on the ADDC deserializes the ART addresses from several VMMs, appends a 5-bit VMM geographical address and a BCID timestamp. It then forms and forwards a data packet to the MM Trigger Processor through optical fiber.

On the back-end of the trigger path, lie the NSW Trigger Processors (TP). The NSW TPs are FPGA-based, housed on Advanced Telecommunications Computing Architecture (ATCA) crates and collect trigger primitives from the ADDC and sFEB/PT/Router boards. The TPs quickly calculate centroids using the ART and 6bADC data, interface with each other to remove duplicates and transmit muon trigger segments/candidates to the Sector Logic.

4. Summary/Conclusions

The NSW is a fully redundant tracking and trigger detector system that is being adequately supported by an advanced electronics scheme, designed to serve both sTGC and MM detector technologies at high rates and under a harsh radiation environment. Both the VMM and the ROC ASICs have been designed to operate under the foreseen data rates and L0A/L1A latencies of Phase-II without loss of data, while the GBTx will be able to support the data acquisition given its large bandwidth. On the trigger path, both the sTGC and the MM scheme have been designed to deliver trigger candidates within the specified latency (1025 ns) [1] and with an adequate precision of 1-2 mrad.

References

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