

Upgrade of the ATLAS Monitored Drift Tube Front-end Electronics for the HL-LHC

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The High-Luminosity Large Hadron Collider will increase the sensitivity of the ATLAS experiment to rare physics processes. In order to cope with a 10 times higher instantaneous luminosity compared to the LHC, the trigger system of ATLAS needs to be upgraded. The ATLAS experiment plans to increase the maximum rate capability of the 1st trigger level to 1 MHz at 10 μ s latency. This requires new on- and off-chamber electronics for its muon spectrometer. The planned upgrade of the on-chamber electronics for the ATLAS Muon Drift-Tube (MDT) chambers is described in these proceedings.

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1. The roadmap to High-Luminosity LHC

The Large Hadron Collider (LHC) was designed to deliver proton-proton collisions at a centre-of-mass energy of $\sqrt{s} = 14$ TeV and a luminosity of $1 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. In order to fully exploits the physics potential of the LHC a successive upgrade to $7 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ is planned: In 2019 and 2020, the so-called “long shutdown 2” (LS2), the injectors will be upgraded to allow the LHC to deliver a larger luminosity; the IP region will be upgraded by the installation of new elements including new focusing magnets and crab cavities in the years 2024 to 2026 during the so-called “long shutdown 3” (LS3). The increase of the luminosity from the LHC to the High-Luminosity (HL) LHC by almost an order of magnitude will lead to an increase of particle fluxes by the same amount such that a major upgrade of the LHC experiments for the operation at HL-LHC is required. The topic of these proceedings is the replacement of the front-end electronics of the Muon Drift-Tube (MDT) chambers of the ATLAS muon spectrometer for the operation at the HL-LHC. In order to cope with the increased particle rates, it is planned to increase the maximum rate capability of the 1st trigger level to 1 MHz at 10 μs latency from its present values of 100 kHz and 2.5 μs .

2. The ATLAS muon spectrometer at the HL-LHC

At the LHC the ATLAS muon spectrometer uses three layers of muon chambers operated in a magnetic field created by an air-core toroid system to trigger on muons with high transverse momenta p_T up to a pseudorapidity $|\eta| = 2.4$ and to measure p_T with 4% resolution in a wide momentum range and 10% at $p_T = 1$ TeV up to $|\eta| = 2.7$ [1]. Resistive Plate Chambers (RPC) in the barrel region and Thin Gap Chambers (TGC) in the end-cap regions with excellent time resolution of a few nanoseconds for pp bunch crossing identification, but moderate spatial resolution, are used for the first level trigger. The high muon momentum resolution is achieved by a precise measurement of muon trajectories with Cathode Strip Chambers (CSC) in the inner end-cap disk at large rapidities and Monitored Drift Tube (MDT) chambers in the rest of the spectrometer. These chambers have spatial resolutions better than 40 μm . The ATLAS muon spectrometer will be upgraded in two steps [2].

The ATLAS muon spectrometer is operated in a large background of neutrons and γ rays. In order to cope with background counting rates of up to 15 kHz cm^{-2} the so-called “small wheel” will be replaced by a new small wheel (NSW) with chambers with increased high-rate capability in LS2 [3]. The other muon spectrometer upgrades will be carried out in LS3. In LS3 new thin-gap RPCs will be added to the inner barrel layer to reduce acceptance losses of the barrel muon trigger. To free space for the RPCs MDT chambers will need to be replaced by so-called “sMDT chambers” which are drift-tube chambers with 15 mm diameter tubes instead of 30 mm diameter tubes of the present MDTs. In order to identify muons within the whole acceptance of the upgraded inner detector of $|\eta| \leq 4.0$ it is considered to install a muon tagger close to the beam pipe between the forward calorimeter and the shielding disk of the NSW. Finally the new trigger architecture will require new on- and off-chamber electronics.

3. On-chamber MDT read-out electronics

An MDT chamber is read out in groups of 24 tubes (3×8 or 4×6 depending on the number of

tube layers per multilayer). Hedgehog cards with coupling capacitors are used to collect the signals from the 24 tubes and route them to the active part which consists of three octal Amplifier Shaper Discriminator (ASD) chips and a 24-channel Time-to-Digital Converter (TDC) chip mounted on a mezzanine card. The digitized signals from up to 18 mezzanine cards are collected by a multiplexer, the so-called “Chamber Service Module” (CSM) which sends the data via an optical fibre to the downstream read-out system.

The present TDCs and CSMs are incompatible with the planned first-level trigger rate of the ATLAS experiment of 1 MHz at the HL-LHC and have to be replaced by new TDCs and CSMs which can cope with the requirements of the new trigger system. As the TDCs are on common mezzanine cards with the ASD chips, new mezzanine cards with new ASD and TDC chips will be designed and built for the upgrade ATLAS muon spectrometer.

4. New Amplifier Shaper Discriminator (ASD) chip

The present ASD chip was designed in Agilent 500 nm technology which has become obsolete. For the upgrade of the ATLAS muon spectrometer a new ASD chip was designed in Global Foundries 130 nm CMOS technology [4]. The design of the new chip follows the design of the present chip, but incorporates a fix of a specific design error of the present chip in the output logic. A block diagram of the new ASD chip is presented in Figure 1. The chip has a differential charge sensitive preamplifier, bipolar shaping with ion tail cancellation and a Wilkinson ASD for time-walk corrections to the discriminated signals.

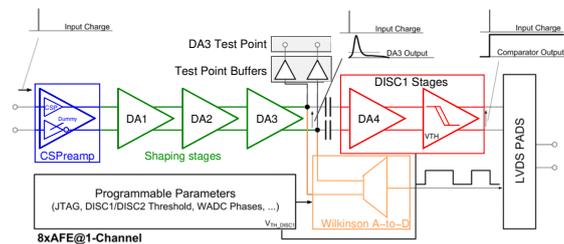


Figure 1: Block diagram of the new ASD chip. [4]

A final version of the new ASD chip has been tested with test pulses and on an MDT chamber in CERN new Gamma Irradiation Facility (GIF++). The new chip supercedes the present chip in terms of smaller peaking time, two times larger amplification, half the noise level and a quarter of the threshold spread at only 10% larger power consumption. The shorter peaking time and the larger amplification of the new chip lead to a better spatial drift-tube resolution than achieved with the present chip.

5. New Time-to-Digital Converter (TDC) chip

Figure 2 shows the block diagram of the new TDC chip which will be designed in 130 nm TSMC CMOS technology. Hit times are measured in coarse steps of 3.125 ns (15 bits) and with an additional fine time in steps of 3.125 ns/4 (2 bits) leading to the target resolution of 0.7815 ns.

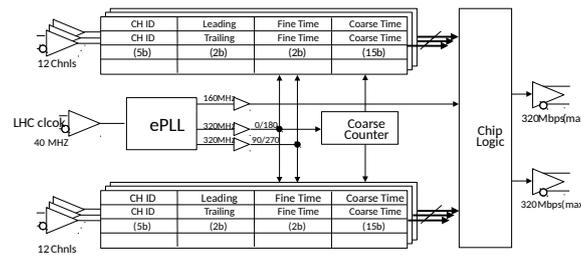


Figure 2: Block diagram of the new TDC chip [5].

A prototype following the same design concept as the new TDC chip was designed in Global Foundries 130 nm CMOS technology and successfully tested confirming the new design concept.

6. New Chamber Service Module (CSM)

The CSM is a multiplexer collecting the data from up to 18 mezzanine cards and sending them downstream via high-speed optical links. It distributes configuration information to the mezzanine cards via down-link and passes monitoring information from mezzanine cards and CSM to the off-detector electronics via up-link. The design of the new CSM must allow for the reuse of the existing cables from the mezzanine cards and provide backward compatibility with legacy mezzanine cards for chambers where these cards are inaccessible for exchange with new cards.

Two design options for the new CSM are under study: a GBTx based CSM which supports CERN's low-power GBT protocol and is radiation hard; an FPGA based CSM which is reprogrammable, but has a limited radiation hardness.

References

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