

Level-1 Track Finding with an All-FPGA System at CMS for the HL-LHC

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The CMS experiment at the LHC is designed to study a wide range of high energy physics phenomena. It employs a large all-silicon tracker within a 3.8 T magnetic solenoid, which in particular allows precise measurements of transverse momentum (p_T) and vertex position.

This tracking detector will be upgraded to coincide with the installation of the High-Luminosity LHC, which will provide a luminosity up to about $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ to CMS, or 200 collisions per 25 ns bunch crossing. This new tracker must maintain the nominal physics performance in this more challenging environment. Novel tracking modules that utilize closely spaced silicon sensors to discriminate on track p_T have been developed that will allow the readout of only hits compatible with $p_T > 2-3 \text{ GeV}$ tracks to off-detector trigger electronics. This will allow the use of tracking information at the Level-1 trigger of the experiment, a requirement to keep the Level-1 triggering rate below the 750 kHz target, while maintaining physics sensitivity.

This article presents a concept for an all FPGA based track finder using a time-multiplexed architecture. Hardware demonstrators have been assembled to prove the feasibility and capability of such a system. The performance for a variety of physics scenarios is discussed, as well as the proposed scaling of the demonstrators to the final system and new technologies.

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By 2026 the LHC [1] will be upgraded in luminosity from about $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ to an expected maximum of $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ [2]. In order for CMS [3] to continue operation, the silicon strip tracker will be replaced during the proceeding long shutdown of the LHC, primarily as a result of radiation damage. A new handle will be needed at the L1 Trigger, in order to keep the rate below the target of 750 kHz, while maintaining thresholds and present sensitivity to interesting physics [4]. For this reason, the new tracker design will read out a sub-set of its data, selected hits from all modules up to $|\eta| < 2.4$, at the bunch crossing rate of 40 MHz.

The new tracker design will use novel *stacked* tracking modules [5], comprising of two 1.6-4.0 mm separated silicon sensors, to discriminate tracks with $p_T > 2 \text{ GeV}$ based on their bend in the CMS magnetic field. In the front-end ASIC, *stubs* are formed from pairs of matched hits, and only these are sent to off-detector trigger electronics at 40 MHz. Each stub includes a strip ID, z-coordinate, and the displacement in strips between the upper and lower sensor hits. This design achieves a rate reduction by about one order of magnitude in comparison to reading out all the hits. The off-detector electronics will then reconstruct tracks from these stubs, providing a new object to the L1 Trigger, that can be used for improved p_T resolution, vertex finding, and track isolation.

1. Track Finding Algorithms and Results

A variety of FPGA-based track finding and reconstruction algorithms are being explored for use in CMS. One of these is the Hough transform [6], a widely used feature extraction technique. In a tracking context, it transforms measured information in pattern space (hits, stubs) to constraints in feature space (track parameters). Clusters or density maxima in the feature space correspond to track candidates. An implementation of this algorithm has been developed in FPGA firmware, and validated in hardware. This implementation of the Hough transform searches for primary tracks in the $r - \phi$ plane, using the parameter ϕ_0 , and the free parameter q/p_T [7, 8]. Stub positions in $r - \phi$ space correspond to straight lines in Hough space. High p_T charged particles are expected to generate stubs in a minimum of six tracking layers. To account for potential inefficiencies, a track candidate is found when four or more lines intersect at a point (or in firmware a cell in an array with a defined granularity). The Hough transform is able to reduce about 12,000 stubs per event down to about 270 track candidates within $1 \mu\text{s}$.

An alternative algorithm generates seeds called *tracklets* [9], formed from pairs of stubs in adjacent tracker layers. This seeding is performed in multiple layer/disk pairs in parallel to build in redundancy. The tracker is divided into 9-27 sectors in ϕ , where each one is further divided into virtual modules in ϕ , each covering the full range in $|\eta|$. To ease routing requirements, only pairs of virtual modules that are consistent with the path of a $p_T > 2 \text{ GeV}$ track are connected. The trajectory defined by the tracklet and the interaction point are extrapolated to virtual modules in the other layers, where matching stubs are identified. A linearised χ^2 fit is performed to calculate the track parameters using the residuals between the tracklet projection and the stubs it has matched. Any calculations required are pre-computed and stored in look-up tables. This algorithm has been demonstrated in hardware with a latency of 2-3 μs .

The Kalman filter [10] is an iterative algorithm that uses a series of measurements containing inaccuracies and noise to produce estimates of unknown variables. Here it is designed to be deployed following the Hough transform, or tracklet algorithms, to clean and precisely fit the track

candidates. The implementation proceeds as follows: an initial estimate of a track's parameters and their uncertainties is taken from either the Hough transform, or tracklet seeds; stubs that belong to the track candidate are added iteratively to the state, whereby the state is updated using a weighted average method that accounts for the uncertainties in the stub measurements, and the earlier track parameter estimates. At each stage in the update, the χ^2 of the track is calculated, and used to reject incorrect stubs and false candidates. In hardware, each iteration takes about 150 ns.

The above algorithms have been demonstrated in hardware, using custom MicroTCA processing boards equipped with Xilinx Virtex-7 FPGAs [11]. Simulated physics events emulating conditions at the HL-LHC are injected into chains of these boards, where the output is captured and compared directly with software emulation. Both algorithm options have very similar tracking performance. The track finding efficiency for $t\bar{t}$ events is shown in Fig. 1 (left). An average efficiency above 95% is measured in emulation for $t\bar{t}$ inclusive tracks above 3 GeV in 200 pileup. In these events around 70 and 200 tracks are reconstructed on average above 3 and 2 GeV, respectively, with a *fake* rate (the fraction of tracks produced that were not constructed entirely from stubs generated by a particle of interest) of about 10%. For the track parameters z_0 and p_T , resolutions of around 1 mm and 1%, respectively, are measured in the tracker barrel. Efficiency for muons is around 99% throughout the tracker. The efficiency for electrons is about 90% above 10 GeV. The algorithms have been demonstrated to have no significant degradation in performance up to 300 pileup, including fake track rate, applying the same latency constraints on processing time as for 200 pileup. These tracks have also been shown to improve pileup rejection and allow vertex finding and application of the particle flow algorithm at the Level 1 Trigger [12].

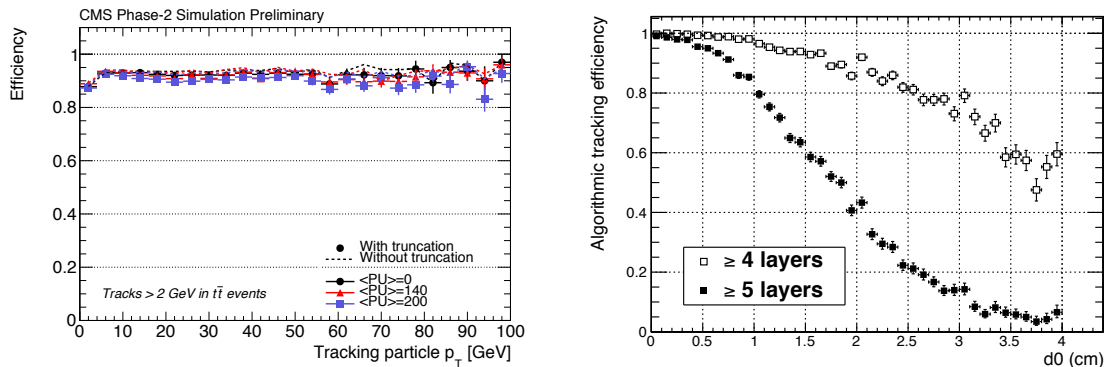


Figure 1: (left) Overall tracking efficiency for all particles with $p_T > 2$ GeV in $t\bar{t}$ events with a pileup of 0, 140, and 200 interactions, using the tracklet algorithm. (right) Hough transform tracking efficiency for displaced single muon particles, with requirements for stubs in either four or five layers. It can be seen that relaxing the requirement to four layers is needed to reconstruct tracks with d_0 greater than about 1 cm.

Finding displaced tracks with a transverse impact parameter, $d_0 < 10$ cm is under investigation [13]. Adaptations are required to the described algorithms. To minimize increases in resource utilization, the objective is to develop a single tracking algorithm that can find both prompt and displaced tracks. The size of Hough transform cells must be increased in order to account for the removal of the beam spot constraint. The requirement on the minimum number of stubs used to form a track must be reduced from five to four, as displaced tracks are less likely to generate stubs

in the innermost layers of the tracker, as they appear as low p_T to the front end. This is shown in Fig. 1 (right). The tracklet algorithm must seed with triplets of stubs, rather than doublets, as the interaction point cannot be used as a third point on the trajectory. Both the Kalman and χ^2 fitters must fit d_0 in addition to p_T , η , ϕ and z_0 . These changes come with increased processing requirements when compared to the prompt track finding designs. A higher fake track rate is expected as a result of removing the beam spot constraint.

2. Summary

To maintain performance at HL-LHC pileup conditions, CMS requires tracks to be used at the Level 1 Trigger. Highly flexible and scalable track finding algorithms have been demonstrated with currently available FPGA processing boards. This demonstration indicates that an FPGA-only Level 1 Track Trigger is a feasible and safe solution for CMS. The inherent flexibility of this design enables adaptation to new physics-driven trigger requirements, such as displaced tracking. Over the next several years, these algorithms will continue to be improved and optimized.

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