Level-1 Calorimeter Trigger: From Virtex-7 to UltraScale+

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With the restart of the LHC in 2021 the ATLAS experiment has to cope with high-luminosity beams. Therefore, a new Level-1 Calorimeter Trigger system will be introduced exploiting a finer calorimeter readout granularity. The new system consists of three Feature EXtractors (FEXs) - electron FEX (eFEX), jet FEX (jFEX) and global FEX (gFEX) - that use FPGAs to reconstruct different physics objects used for the trigger selection and that gather data from the calorimeters through optical fibres. The Trigger Objects (TOBs) produced by the algorithms running on the FEXs are optically sent to the Level-1 Topological Processor (L1Topo), where interesting physics events are selected by e.g. applying kinematic and angular requirements.

This contribution will focus on the new jFEX system and on the upgrade of the L1Topo giving an overview of the hardware as well as the algorithmic firmware.

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1. Introduction & Motivation

The Level-1 Topological Processor (L1Topo) is part of the ATLAS Level-1 Trigger since the first upgrade period (2013 to 2015) during Long Shutdown 1 (LS1). With L1Topo it became possible for the first time to transfer 4-vectors of all Trigger Objects (TOBs) for the full event to a single module and process them with FPGAs. Before, Level-1 Trigger decisions were taken only from multiplicities (for several p_T thresholds).

During Long Shutdown 2 (2019 and 2020) the Large Hadron Collider (LHC) will be upgraded to an instantaneous luminosity of about $2.5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ corresponding to an average number of interactions per bunch crossing of about 60. To cope with these new conditions several upgrades of the ATLAS Trigger and Data Acquisition system (TDAQ) have been planned. As part of this, the Level-1 Calorimeter Trigger will include the new sub-system called jet Feature EXtractor (jFEX). The jFEX system is intended to identify jets with and without substructure and taus, as well as to calculate the total transverse energy sum and missing transverse energy.

In addition, L1Topo has been redesigned to meet the new requirements, e.g. an increased input bandwidth (more links, higher data rates) and many more logic resources to be able to run more complex algorithms.

2. The Level-1 Topological Processor during Run-2

The L1Topo system during Run-2 consists of 2 ATCA boards (modules). Each module hosts 2 Xilinx Virtex-7 FPGAs for event processing and 1 Xilinx Kintex-7 FPGA for control and readout. A picture of the L1Topo module is shown in Figure 1.
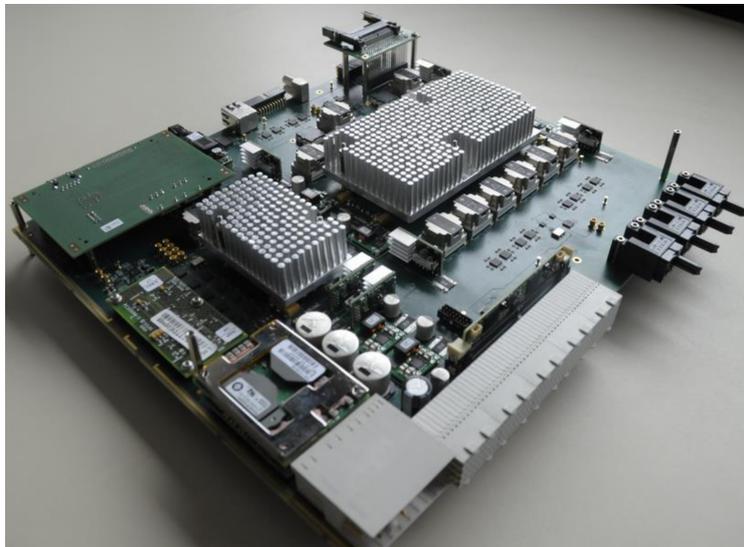

Figure 1: L1Topo Module during Run-2. The FPGAs are covered by heat sinks.

Each processor FPGA receives different types of Trigger Objects (TOBs), e.g. 4-vectors of muons, electrons, taus and jets, from the calorimeter and muon triggers through 80 multi-gigabit receivers running at a link speed of 6.4 Gb/s. Therefore, a total data rate of about 1 Tb/s with a latency budget of 150 ns is being processed by a single module.

The L1Topo firmware algorithms are configurable and being executed in 75 ns. During this time, up to 128 algorithms in use are calculating event topological variables, e.g. angular distances, transverse and invariant masses. Physics running has shown, that with an integrated L1Topo system a significant reduction of background rates can be achieved while keeping a good signal efficiency without raising E_T thresholds. More details are given in Ref. [1].

Finally, L1Topo provides trigger decisions to the Central Trigger Processor, which sends out the Level-1 accept.

3. Upgrades of the Level-1 (Calorimeter) Trigger towards Run-3 and beyond

3.1 jet Feature EXtractor (jFEX)

The jFEX system is going to replace the Jet / Energy Modules (JEMs), which were mainly responsible for jet identification inside the Level-1 Trigger during Run-1 and Run-2. To cover the full calorimeter, the entire jFEX system runs on 6 ATCA boards (modules). 4 Xilinx UltraScale+ FPGAs for processing and an Avnet UltraZed EV board as a control mezzanine are placed on each module. A picture of the jFEX prototype is shown in Figure 2a.
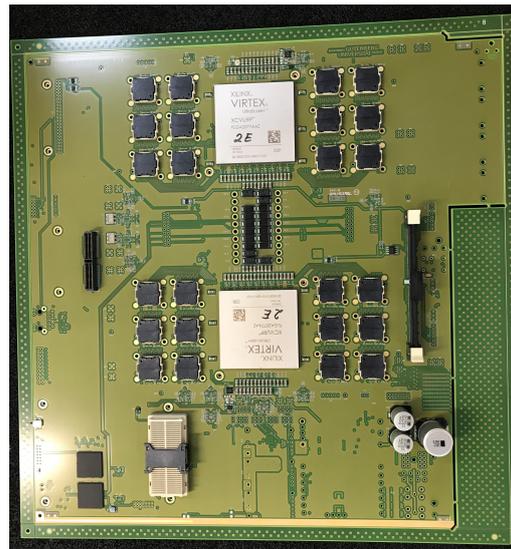
(a) jFEX prototype.   (b) Upgraded L1Topo prototype.

Figure 2: Pictures of the (a) jFEX prototype and (b) upgraded L1Topo prototype. All processor FPGAs are visible, while the control mezzanines are not shown in these pictures.

The ATCA board consists of 24 layers (including ground layers) of MEGTRON6, chosen because of its low dielectric constant (low attenuation). The PCB layout was accompanied and checked by power, thermal and signal integrity simulations to minimize voltage drops and to avoid thermal hotspots.

120 multi-gigabit transceivers (MGTs) per FPGA are running at link speeds of up to 12.8 Gb/s. Link speed tests were run at such line rates to a bit error rate of better than 1×10^{-15} without seeing a single error. The measured power consumption, while all MGTs are enabled, is about 266 W and

therefore well within the limits of ATCA standard (400 W). In addition, measurements of thermal propagation were performed without seeing any critical temperatures.

Each module has to deal with a total input bandwidth of approximately 3 Tb/s with a latency budget of less than 400 ns.

The jFEX firmware algorithms have a maximum processing time of 150 ns. Most of the algorithms have been implemented and successfully tested on hardware, e.g. event-by-event and η dependent pile-up calculation and subtraction, identification of jets, calculation of the total transverse energy sum and missing transverse energy, generation and sorting of TOBs. Algorithms for jets with substructure and taus are currently being studied.

Performance studies have shown a significant improvement of the jFEX jet identification algorithm (based on the *sliding window* algorithm) compared to the Run-2 system.

3.2 Upgraded Level-1 Topological Processor (Upgraded L1Topo)

The upgraded L1Topo is based on the jFEX hardware. In total, 3 modules are required, each equipped with 2 Xilinx UltraScale+ FPGAs for processing. A single FPGA has 118 input and 24 output fibres running at up to 12.8 Gb/s. A picture of the prototype is shown in Figure 2b.

Through the upgrade from Xilinx Virtex-7 FPGAs to the new UltraScale+ devices, about three times more logic resources become available, which leads to room for multiplicity algorithms and even more complex ones.

4. Conclusions & Outlook

In 2021 the LHC will be able to deliver data at high luminosity and an increased event rate. Thus, upgrades of the ATLAS Level-1 Trigger system are necessary. jFEX is one of the new subsystems mainly responsible for jet identification, while the L1Topo system needs to be upgraded to meet the new requirements.

The jFEX and upgraded L1Topo are new boards based on Xilinx UltraScale+ FPGAs running at a link speed of up to 12.8 Gb/s. It has been shown that the jFEX prototype works reliably in measurments of data transmission, power consumption and thermal propagation. The upgraded L1Topo is based on the jFEX hardware-wise.

The larger FPGAs allow implementations of more complex algorithms. Improvements in performance have been shown in high-level simulations. Therefore, these upgrades will allow to maintain high trigger efficiencies despite the increased luminosity.

The final production of the boards is ongoing. Integration tests are planned at the beginning of 2019 and the installation is scheduled for autumn 2019.

References

[1] ATLAS Experiment, *Trigger Operation Public Results*, `https://twiki.cern.ch/twiki/bin/view/AtlasPublic/TriggerOperationPublicResults`.